JERUSALEM COLLEGE OF ENGINEERING

(An Autonomous Institution)

(Approved by AICTE, Affiliated to Anna University,
Accredited by NBA and NAAC with 'A' Grade)
Velachery Main Road, Narayanapuram, Pallikaranai, Chennai - 600100

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION OF THE INSTITUTION

Jerusalem College of Engineering is committed in emerging as an international institution of excellence in imparting finest quality engineering, technology and management education rooted in ethical and societal values through various academic programmes, multi-disciplinary research, consultancy and entrepreneurship activities and hence to contribute towards social transformation and nation building.

MISSION OF THE INSTITUTION

- Generating abundant resources and making conducive policies, the management led by the Chief Executive Officer strives towards promoting globally competitive academic programmes augmented with value added courses, in-plant training activities, co-curricular activities and ambience that support intellectual growth and skill acquisition

- Promoting collaborative trans-border research programmes continuing education in synergy with academia, industries and research organizations leading to real time solutions and life-long learning

- Transforming young men and women into competent professionals and entrepreneurs motivated by a passion for professional excellence, driven by human values and proactively engage in the betterment of the society through innovative practices and academic excellence

- Facilitating effective interaction among faculty members and students and fostering network of alumni, industries, institutions and other stake-holders for successful career gain and placement

VISION OF THE DEPARTMENT

The Department of Electronics and Communication Engineering is committed to promote academic excellence and research to meet the needs of society and International Industrial requirements and standards.

MISSION OF THE DEPARTMENT

- To equip the graduates to be competent with excellent knowledge through innovative teaching methods.

- To promote relevant academic excellence through value added courses.

- To train the graduates in qualitative and quantitative skills in research to meet the International Industrial standards.

- To inculcate ethical values and social consciousness among the graduates to enrich themselves and also the community as a whole.

PROGRAM OUTCOMES (POs)

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area of applied electronics.

PO4: Enhance and develop systems, protocols using modern tools and provide optimal solutions to problem areas in advanced signal processing, embedded systems and VLSI design.

PO5: Apply technical knowledge on fundamentals of applied electronics towards the development of socially relevant eco-friendly products.

PO6: Work with professional and ethical values in the field of applied electronics and related areas.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1: To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.

PEO2: To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.

PEO3: To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.

M.E. APPLIED ELECTRONICS R2021 CREDIT DETAILS

S. No	M.E APPLIED ELECTRONICS						Percentage
	SUBJECT AREA	CREDITS PER SEMESTER				TOTAL CREDITS	
		I	II	III	IV		
1	FC	3	-	-	-	3	**4.29**
2	PC	14	11	-	-	25	**35.71**
3	PE	3	6	6	-	15	**21.43**
4	OE	-	-	3	-	3	**4.29**
5	EEC	-	3	9	12	24	**34.29**
TOTAL CREDITS		**20**	**20**	**18**	**12**	**70**	**100.00**

JERUSALEM COLLEGE OF ENGINEERING
(AN AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI)
M.E. APPLIED ELECTRONICS
REGULATION 2021
CHOICE BASED CREDIT SYSTEM
I TO IV SEMESTERS CURRICULUM AND SYLLABI

SEMESTER 1

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	JMA5102	Applied Mathematics	FC	3	3	0	0	3
2	JAE5101	Advanced Digital System Design	PC	3	3	0	0	3
3	JAE5102	Embedded System Design	PC	3	3	0	0	3
4	JAE5103	RTL Simulation and Synthesis with PLDs	PC	4	4	0	0	4
5		Professional Elective 1	PE	3	3	0	0	3
6		Non Credit Mandatory Course 1	NCM	2	2	0	0	0
PRACTICALS								
7	JAE5111	Embedded System Design Laboratory	PC	4	0	0	4	2
8	JAE5113	RTL Simulation and Synthesis with PLDs Laboratory	PC	4	0	0	4	2
TOTAL				**26**	**18**	**0**	**8**	**20**

SEMESTER 2

S. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	JAE5201	Analog and Digital CMOS VLSI Design	PC	3	3	0	0	3
2	JAE5202	Advanced Digital Signal Processing	PC	3	3	0	0	3
3	JAE5203	Computer Vision	PC	3	3	0	0	3
4		Professional Elective 2	PE	3	3	0	0	3
5		Professional Elective 3	PE	3	3	0	0	3
6		Non Credit Mandatory Course 2	NCM	2	2	0	0	0
PRACTICALS								
7	JAE5211	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2
8	JAE5241	Mini Project	EEC	4	0	0	4	2
9	JAE5251	Term Paper Writing and Seminar	EEC	2	0	0	2	1
TOTAL				**35**	**15**	**4**	**16**	**20**

SEMESTER 3

S. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1		Professional Elective 4	PE	3	3	0	0	3
2		Professional Elective 5	PE	3	3	0	0	3
3		Open Elective 1	OE	3	3	0	0	3
4	JRM5301	Research Methodology and IPR	EEC	2	2	0	0	2
PRACTICALS								
5	JAE5361	Project Work - Phase 1	EEC	12	0	0	12	6
6	JAE5321	Technical Seminar	EEC	2	0	0	2	1
TOTAL				**25**	**11**	**0**	**14**	**18**

SEMESTER 4

S. No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1	JAE5461	Project Work – Phase 2	EEC	24	0	0	24	12
TOTAL				**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 70

PROFESSIONAL ELECTIVES – 1
Semester I

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5001	Sensors, Actuators and Interface Electronics	PE	3	3	0	0	3
2	JAE5002	Analog Integrated Circuit Design	PE	3	3	0	0	3
3	JAE5003	MEMS Based Devices	PE	3	3	0	0	3
4	JAE5004	Advanced Microprocessors and Microcontrollers	PE	3	3	0	0	3

PROFESSIONAL ELECTIVES – 2
Semester II

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5005	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3
2	JAE5006	Testing of VLSI Circuits	PE	3	3	0	0	3
3	JAE5007	RF System Design	PE	3	3	0	0	3
4	JAE5008	VLSI Signal Processing	PE	3	3	0	0	3

PROFESSIONAL ELECTIVES – 3
Semester II

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5009	Internet of Things	PE	3	3	0	0	3
2	JAE5010	Nanomaterials and Nanotechnology	PE	3	3	0	0	3
3	JAE5011	EMI and EMC in System Design	PE	3	3	0	0	3
4	JAE5012	Pattern Recognition	PE	3	3	0	0	3

PROFESSIONAL ELECTIVES – 4
Semester III

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5013	Voice and data networks	PE	3	3	0	0	3
2	JAE5014	Artificial Intelligence and Machine Learning	PE	3	3	0	0	3
3	JAE5015	DSP Integrated Circuits	PE	3	3	0	0	3
4	JAE5016	Robotics and Intelligent Systems	PE	3	3	0	0	3

PROFESSIONAL ELECTIVES – 5
Semester III

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5017	Cognitive Networks	PE	3	3	0	0	3
2	JAE5018	Computer Architecture and Parallel Processing	PE	3	3	0	0	3
3	JAE5019	Digital System Testing and Testable Design	PE	3	3	0	0	3
4	JAE5020	Computer Network Security	PE	3	3	0	0	3

OPEN ELECTIVES - 1

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE9001	Wearable Technology and Applications	OE	3	3	0	0	3
2	JAE9002	Industrial Safety	OE	3	3	0	0	3
3	JAE9003	Introduction to VLSI Technology	OE	3	3	0	0	3
4	JAE9004	Introduction to Embedded Controllers	OE	3	3	0	0	3
5	JAE9005	Automotive Electronics	OE	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JAE5241	Mini Project	EEC	4	0	0	4	2
2	JAE5251	Term Paper Writing and Seminar	EEC	2	0	0	2	1
3	JAE5321	Technical Seminar	EEC	2	0	0	2	1
4	JMR5301	Research Methodology and IPR	EEC	3	0	0	2	2
5	JAE5361	Project Work - Phase – 1	EEC	2	0	0	2	6
6	JAE5461	Project Work – Phase -2	EEC	24	0	0	24	12

NON CREDIT MANDATORY COURSES (NMC)

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	JNC5001	English for Research Paper Writing	NCM	2	2	0	0	0
2	JNC5002	Disaster Management	NCM	2	2	0	0	0
3	JNC5003	Sanskrit for Technical Knowledge	NCM	2	2	0	0	0
4	JNC5004	Value Education	NCM	2	2	0	0	0
5	JNC5005	Constitution of India	NCM	2	2	0	0	0
6	JNC5006	Pedagogy Studies	NCM	2	2	0	0	0
7	JNC5007	Stress Management by Yoga	NCM	2	2	0	0	0
8	JNC5008	Personality Development through Life Enlightenment Skills	NCM	2	2	0	0	0
9	JNC5009	Unnat Bharat Abhiyan	NCM	2	2	0	0	0

SEMESTER 1

JMA5102	APPLIED MATHEMATICS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To develop the ability to apply the concepts of Fuzzy Algebra.
- To explain the concepts of Matrix Theory in decomposition problems.
- To elucidate problem solving through various methods in Linear Programming.
- To familiarize the students in various concepts and methods in Calculus of Variations.
- To enable students to understand Multivariate Analysis and its applications.

UNIT I FUZZY SETS AND LOGIC 9

Fuzzy sets – Properties and Operations – Fuzzy relations – Operations on Fuzzy relations - Classical logic – Multivalued logic – Fuzzy propositions – Fuzzy quantifiers

UNIT II MATRIX THEORY 9

The Cholesky decomposition - Generalized Eigen vectors, Canonical basis - QR factorization -Least squares method - Singular value decomposition

UNIT III LINEAR PROGRAMMING 9

Formulation – Graphical solution – Simplex method – Big M method –Two phase method – Transportation and Assignment Models – Dynamic Programming

UNIT IV CALCULUS OF VARIATIONS 9

Concept of variation and its properties – Euler's equation – Functionals dependent on first and higher order derivatives – Functionals dependent on functions of several independent variables– Problems with constraints– Ritz Method

UNIT V MULTIVARIATE ANALYSIS 9

Random vectors and Matrices – Mean vectors and Covariance matrices – Multivariate Normal density and its properties – Principal components: Population principal components – Principal components from standardized variables

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course students will be able

- To apply multivalued logic and fuzzy logic in problems
- To use matrix theory in practical applications and problem solving
- To solve linear programming problems through simplex and two phase methods and understand LP extensions: Transportation and Assignment Models
- To solve problems based on calculus of variations in engineering applications and get exposed to standard methods
- To understand multivariate analysis and use Principal Component Analysis in problems

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and Fuzzy Logic, Theory and Applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Richard Bronson, "Matrix Operations", Schaum's outline series, 2nd Edition, McGraw Hill, 2011.
3. Taha, H.A., "Operations Research, An introduction", 10th edition, Pearson education, New Delhi, 2010.
4. Gupta, A.S., Calculus of Variations with Applications, Prentice Hall of India Pvt. Ltd., NewDelhi, 1997.
5. Elsgolts, L., Differential Equations and the Calculus of Variations, MIR Publishers, Moscow,1973.
6. Richard A.Johnson and Dean W.Wichern, "Applied Multivariate Statistical Analysis", Pearson Education, Asia, 6th Edition, 2007

WEBSITE REFERENCES:

1. https://nptel.ac.in/courses/108/104/108104157/
2. https://nptel.ac.in/courses/111/107/111107112/
3. https://nptel.ac.in/courses/111/102/111102012/
4. https://nptel.ac.in/courses/111/104/111104025/
5. https://nptel.ac.in/courses/111/104/111104024/

CO-PO MAPPINGS

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	-	-
CO2	3	3	2	2	-	-
CO3	3	3	2	2	-	-
CO4	3	3	2	2	-	-
CO5	3	3	2	2	-	-
AVG	3	3	2	2	-	-

JAE5101	**ADVANCED DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- Introduce methods to analyse and design synchronous sequential circuits
- Introduce methods to analyse and design a synchronous sequential circuits and to analyse hazards
- Introduce the fault testing procedure for combinational circuits and PLA circuits
- Introduce the architectures of programmable devices
- Introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state tableassignmentandreduction-Designofsynchronoussequentialcircuitsdesignofiterativecircuits-ASMchartandrealizationusingASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit — flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards — mixed operating mode asynchronous circuits —designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method -D algorithm –Kohavi algorithm — Tolerance techniques — The compact algorithm — Fault in PLA — Test generation-DFT schemes–Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families–Designing asynchronous sequential circuit using PLA/PAL – Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx4000- Versal AI Core VC1902

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL- Behavioural Descriptions in Verilog HDL–HDL Based Synthesis–Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog –Registers — counters — sequential machine — serial adder — Multiplier- Divider — Design of simple microprocessor

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- Analyse and design synchronous sequential circuits
- Analyse hazards and design asynchronous sequential circuits
- Knowledge on the testing procedure for combinational circuit and PLA
- Able to design PLD and ROM
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.Roth Jr, “Fundamentals of Logic Design”, Thomson Learning,2004.
2. M.D.Ciletti , “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PrenticeHall,1999.
3. M.G.Arnold,“VerilogDigital–ComputerDesign”,PrenticeHall(PTR),1999.
4. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India,2001.
5. Parag K.Lala, “Fault Tolerant and Fault Testable Hardware Design”, BS Publications,2002.
6. ParagK.Lala, “Digital system Design using PLD”, BS Publications, 2003.
7. S.Palnitkar, “Verilog HDL–A Guide to Digital Design and Synthesis”, Pearson,2003.

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1. www.nptel.ac.in
2. https://www.xilinx.com/products/boards-and-kits/vck190.html
3. http://www.wseas.us/e-library/transactions/electronics/2008/32-252.pdf
4. https://nptel.ac.in/courses/108/106/108106177/
5. https://nptel.ac.in/courses/117/108/117108040/

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	2	1	1	1
CO2	1	1	2	1	1	1
CO3	3	1	1	3	1	1
CO4	1	1	1	1	2	1
CO5	1	1	1	2	1	2
AVG	1.4	1	1.4	1.6	1.2	1.2

JAE5102	EMBEDDED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To expose the students to the fundamentals of embedded system design.
- To enable the students to understand and use embedded computing platform.
- To introduce networking principles in embedded devices.
- To learn real time characteristics in embedded system design.
- To explore system design techniques.

UNIT I EMBEDDED PROCESSORS 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges inEmbeddedComputingsystemdesign,Embeddedsystemdesignprocess-Requirements,Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Design Example: Model Train Controller, ARM processor- processor and memory organization, Case study: Smart Card.

UNIT II EMBEDDED COMPUTING PLATFORM 9

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example: Alarm Clock, Case Study: Face Recognition system.

UNIT III NETWORKS 9

DistributedEmbeddedArchitecture-HardwareandSoftwareArchitectures,Networksforembedded systems- I^2C, CAN Bus, USB, Ethernet, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11, Network Based design Communication Analysis, system performance Analysis, Hardware platform design, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS 9

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, Off-line Versus On-line scheduling. Design Example: Engine control unit, Case Study: Automatic Chocolates Vending Machine.

UNIT V SYSTEM DESIGN TECHNIQUES 9

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Examples: Telephone PBX- System Architecture, Ink jet printer-Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes, Video accelerator.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- To explore fundamentals of embedded system design.
- To interpret and use embedded computing platform.
- To apply networking principles in embedded devices.
- To gain insight on the real time characteristics of an embedded system design.
- To understand embedded system design techniques.

REFERENCES:

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 3rdEdition, 2012.
2. Jane.W.S.Liu, "Real-Time systems", Pearson Education Asia, 2001.
3. C.M.Krishna and K.G.Shin, "Real-Time Systems" ,McGraw-Hill,1997.
4. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/ Software Introduction", John Wiley &Sons,2002.
5. Jane W.S.Liu, Real Time Systems‖, Pearson Education, Third Indian Reprint, 2003.

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2. https://nptel.ac.in/courses/108/102/108102169/Dhananjay V.Cadre, IIT Jammu.
3. https://nptel.ac.in/courses/108/102/108102045/Prof. Santanu Chaudhary, Department of Electrical Engineering, IIT Delhi.
4. http://www.nptelvideos.in/2012/11/embedded-systems.html.
5. https://nptel.ac.in/courses/108/102/108102169/

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO-1	2	2	2	2	1	1
CO-2	3	3	2	3	1	-
CO-3	3	2	2	1	2	-
CO-4	2	3	1	2	3	-
CO-5	3	3	2	3	2	-
AVG	2.6	2.6	1.8	2.2	1.8	1

JAE5103	RTL SIMULATION AND SYNTHESIS WITH PLDs	L	T	P	C
		4	0	0	4

COURSE OBJECTIVES:

- Familiarity in Design Approaches in PLDs
- Familiarity of Finite State Machines, RTL design using HDL.
- Familiarity of ASIC Design
- Understand the performance of VLSI circuits
- Design and develop IP cores and Prototypes with performance guarantees

UNIT I DESIGN APPROACH 9

Top-down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT II DIGITAL DESIGN USING HDL 9

Importance of HDL- types-Modelling types, tasks, functions, delay. Design of combinational and sequential circuits, FSM and implementation using FSM, Realization of State Machines.

UNIT III ASIC DESIGN FLOW 9

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

UNIT IV POWER AND PERFORMANCE 9

Design for performance - Low power VLSI design techniques- power optimization- synthesis for low power.

UNIT V IP AND PROTOTYPING 9

IP in various forms: RTL Source code, Encrypted Source code, SoftIP, Netlist, Physical IP, Use of external hard IP during prototyping

Casestudies: Canonical Signed Digit Arithmetic, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- Familiar in Finite State Machines, RTL design.
- Familiar in design using HDL
- Able to explain ASIC Design
- Understand the concepts of Power in VLSI circuits
- Design and develop IP cores and Prototypes with performance guarantees

REFERENCES:

1. Richard S.Sandige, “Modern Digital Design”, MGH, International Editions.
2. DonaldD Givone, “Digital principles and Design”, TMH
3. Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning
4. SamirPalnitkar,“VerilogHDL,aguidetodigitaldesignandsynthesis”,PrenticeHall.
5. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
6. Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008
7. BobZeidman, “Designing with FPGAs & CPLDs”, CMP Books.

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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	2	1	1	1
CO2	1	1	2	1	1	2
CO3	2	3	2	3	2	1
CO4	2	3	2	1	2	1
CO5	2	3	2	2	3	2
AVG	1.6	2.4	2	1.6	1.8	1.4

JAE5111	EMBEDDED SYSTEM DESIGN LABORATORY	L	T	P	C
		0	0	4	2

COURSE OBJECTIVES:

- To learn asynchronous and clocked synchronous sequential circuits
- To understand the concept of built-in self-test and fault diagnosis
- To understand testing RTOS environment and system programming
- To learn wireless network design using embedded systems
- To know use of Verilog and VHDL in sequential digital system modeling

LIST OF EXPERIMENTS

1. System design using PIC, MSP430,8051Microcontroller and16-bit Microprocessor 8086.
2. Implementation of Adaptive Filters and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Analysis of Asynchronous and clocked synchronous sequential circuits
5. Built in self test and fault diagnosis
6. Sensor design using simulation tools
7. Design and analysis of real time signal processing system– Data acquisition and signal processing
8. Testing RTOS environment and system programming
9. Designing of wireless network using embedded systems
10. Implementation of ARM with FPGA
11. Flash controller programming - data flash with erase, verify and fusing

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- ApplyPIC,MSP430,8051Microcontrollerand8086forsystemdesign
- Simulate QMF
- Design sensor using simulation tools
- Design and analyze of real time signal processing system
- Assess flash controller programming- data flash with erase, verify and fusing

WEBSITE REFERENCES:

1. https://nptel.ac.in/courses/117/108/117108140/PROF.NV CHALAPATHI RAO Department of Electrical and Electronic Engineering IISc Bangalore.
2. https://nptel.ac.in/courses/117/106/117106111/S.Chandramouleeswaran, Department of Electronics and communication Engineering
3. https://nptel.ac.in/courses/117/106/117106086/
4. https://nptel.ac.in/course.html
5. https://www.vlab.co.in/broad-area-electronics-and-communications

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	2	1	2	2
CO2	2	2	2	3	3	3
CO3	2	2	2	3	3	2
CO4	3	2	2	1	2	3
CO5	3	2	2	3	2	1
AVG	2.4	2.2	2	2.2	2.4	2.2

JAE5113	**RTL SIMULATION AND SYNTHESIS WITH PLDs LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

COURSE OBJECTIVES:

- Identify, formulate, solve and implement problems in signal processing using RTL design tools.
- Identify, formulate, solve and implement problems in communication systems using RTL design tools.
- Verilog implementation of digital circuits
- Validate the design in FPGA
- Use Xilinx tool.

LIST OF EXPERIMENTS:

1. Verilog implementation of 8:1 Mux/ Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2. Sequence generator/detectors, Synchronous FSM–Mealy and Moore machines.
3. Traffic Light controller, elevator control.
4. PCI Bus & arbiter.
5. UART/USART using Verilog.

6. Verilog implementation of Arithmetic circuits like serial adder / subtractor, parallel adder / subtractor, serial / parallel multiplier.
7. Discrete Fourier transform/ Fast Fourier Transform algorithm in Verilog.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- Identify, formulate, solve and implement problems in signal processing using RTL design tools.
- Identify, formulate, solve and implement problems in communication systems using RTL design tools.
- Implement digital circuits using FPGA
- Validate the design in FPGA.
- Use the EDA tools like Xilinx

WEBSITE REFERENCES:-

1. https://in.mathworks.com/solutions/fpga-asic-soc-development/xilinx.html
2. https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm
3. https://www.javatpoint.com
4. https://www.vlab.co.in/broad-area-electronics-and-communications
5. https://www.digimat.in/nptel/courses/video/117108040/L01.html

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	3	3	2	1
CO2	1	1	3	3	2	1
CO3	1	1	3	3	2	1
CO4	1	1	3	2	2	1
CO5	1	1	3	2	2	1
AVG	1	1	3	2	2	1

SEMESTER 2

JAE5201	ANALOG AND DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand design and operation of basic analog circuits.
- Design principles and techniques for analog IC's blocks implemented in CMOS technology.
- To introduce the transistor level design of all digital building blocks.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.
- To learn about the memory organization and arithmetic building blocks.

UNIT I ANALOG CMOS SUB-CIRCUITS 9

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT II CMOS AMPLIFIERS & OPERATIONAL AMPLIFIERS 9

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, High Gain Amplifiers Architectures. Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps.

UNIT III MOSTRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary effects, CMOS Inverter Static Characteristic, Dynamic Characteristic, Power, Energy parameters, Stick diagram and Layout diagrams.

UNIT IV COMBINATIONAL & SEQUENTIAL LOGIC CIRCUITS 9

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Dynamic Logic Gates. Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines.

UNIT V MEMORY & ARITHMETIC BUILDING BLOCKS 9

Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell.

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course students will be able to:

- Be well versed with the analog CMOS subcircuits.
- Analyze and design analog circuits such as Differential Amplifier, OP-AMP, Current mirrors, Biasing circuits.
- Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits
- Create models of moderately sized static CMOS combinational circuits and to design sequential logic at the transistor level and Compare the tradeoffs of sequencing elements.
- Learn design methodology of arithmetic building blocks and functional units including ROM and SRAM

REFERENCES:

1. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International 2nd Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley India, 5th Edition, 2010.
3. JanRabaey, Anantha Chandrakasan, BNikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India", 2nd Edition, Feb 2003.
4. David A. Johns, Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2013.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition.
6. Baker, Li and Boyce, "CMOS: Circuit Design, Layout and Simulation", PHI.
7. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993.
8. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.
9. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill, 1998.

WEBSITE REFERENCES:

1. https://nptel.ac.in/courses/117/101/117101105/, Prof. A.N. Chandorkar, IIT Bombay.
2. https://nptel.ac.in/courses/108/107/108107129/, Prof. Sudeb Dasgupta, IIT Roorkee.
3. https://www.youtube.com/watch?v=tAkycQ-UdS0, Prof. Goutam Saha, IIT Kharagpur.
4. https://www.youtube.com/watch?v=oL8SKNxEaHs, CMOS Digital VLSI
5. https://www.youtube.com/watch?v=3p_tGqCu8Ds, Introduction to CMOS Analog VLSI

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	2	1
CO2	3	3	3	3	3	2
CO3	2	3	3	3	3	2
CO4	3	3	2	3	3	1
CO5	3	3	3	2	3	2
AVG	2.8	3	2.8	2.6	2.8	1.6

JAE5202	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- comprehends mathematical description and modelling of discrete time random signals.
- learns relevant figures of merit such as power, energy, bias and consistency.
- conversant with important theorems and random signal processing algorithms
- familiarize with estimation, prediction, filtering.
- Understand the applications of multirate signal processing concepts and techniques

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete random processes–Ensemble averages– Wide sense stationary process– Properties- Ergodic process – Sample mean & variance - Auto-correlation and Auto-correlation matrices- Properties – White noise process – Weiner Khitchine relation - Power spectral density – Filtering random process–Spectral Factorization Theorem.

UNIT II SPECTRUM ESTIMATION

9

Bias and Consistency of estimators- **Non-Parametric methods**: Periodogram, Modified Periodogram, Barlett's method, Welch's method, Blackman-Tukey method-**Parametric Methods:** AR, MA, ARMA Processes and spectrum estimation, Yule-Walker equations, Burg estimation algorithm Performance analysis of estimators.

UNIT III SIGNAL MODELING AND OPTIMUM FILTERS 9

SIGNAL MODELING: Least square method–Pade approximation–Prony's method–Levinson Recursion

OPTIMUM FILTERS: Lattice filter - FIR Wiener filter – Filtering – Linear Prediction – Non Causal and Causal IIR Weiner Filter -– Mean square error – Discrete Kalman filter, Application of Kalman Filter Model in the Landslide Deformation Forecast.

UNIT IV ADAPTIVE FILTERS 9

FIR Adaptive filters - Newton's steepest descent method – Widrow Hoff LMS Adaptive algorithm –Convergence – Normalized LMS – Applications – Noise cancellation - channel equalization – echo canceller – Adaptive Recursive Filters - RLS adaptive algorithm – Exponentially weighted RLS-sliding window RLS- FEDS AND RAMP: relation to RLS.

UNIT V APPLICATIONS OF MULTI RATE SIGNAL PROCESSING 9

Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Transmultiplexers Application of multirate digital signal processing to image compression.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course students will be able to:

- Formulates time domain and frequency domain description of Wide Sense Stationary process in terms of matrix algebra and relate to linear algebra concepts.
- States W-K theorem, spectral factorization theorem, spectrum estimation, bias and consistency of estimators.
- understands theory of different filters and algorithms
- Analyzes the RLS and LMS algorithms, and its applications
- understand concepts of multirate signal processing application

REFERENCES:

1. John G. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Prentice Hall of India, New Delhi,2005.
2. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons Inc., New York, 2006.
3. P. P.Vaidyanathan, “Multirate Systems and Filter Banks”, Prentice Hall, 1992.
4. Alan V Oppenheim & Ronald W Schaffer, ”Discrete Time signal processing,” PHI.
5. Emmanuel C. Ifeacher, Barrie. W. Jervis, “DSP A Practical Approach” second edition., Pearson Education.
6. Kaluri V. Rangarao, Ranjan K. Mallik , “Digital Signal Processing: A Practitioner's Approach” ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Weley.
7. S.Salivahanan, A.Vallavaraj, C.Gnanapriya ,”Digital Signal Processing “ 2000,TMH
8. S. Kay,” Modern spectrum Estimation theory and application”, Prentice Hall, Englehood Cliffs, NJ1988
9. Simon Haykin, “Adaptive Filter Theory”, Prentice Hall, Englehood Cliffs, NJ1986.
10. Sophoncles J.Orfanidis, “Optimum Signal Processing“, McGraw-Hill,2000.

WEBSITE REFERENCES:

1. https://onlinecourses.nptel.ac.in/noc20_ee53/preview
2. https://nptel.ac.in/noc/courses/noc17/SEM1/noc17-ch03/
3. https://www.youtube.com/watch?v=rTYMfAI8mGE
4. https://nptel.ac.in/courses/117/105/117105075/
5. https://www.youtube.com/watch?v=M8U-oO4SXYk

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	2
CO2	3	3	3	3	2	2
CO3	3	3	3	3	2	3
CO4	3	3	3	3	3	1
CO5	3	3	3	3	3	1
AVG	3	3	3	3	2.4	1.8

JAE5203	**COMPUTER VISION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To solve real world problems with image or video as input, understanding the real world the input.
- To familiarize the feature extraction from the given image and shape analysis
- To understand low level image processing and pattern recognition algorithms
- To understand the design of algorithms to understand real world scene
- To learn applications in many areas such as biometric, medical image diagnosis, surveillance etc.

UNIT I IMAGING SYSTEM 9

Monocular and Binocular imaging system Orthographic & Perspective Projection, Camera model and Camera calibration, Binocular Stereopsis - Epipolar Geometry, Homography, Rectification, DLT, RANSAC 3-D reconstruction framework; Auto-calibration, Apparel, Stereo vision, Vision intelligence for safety

UNIT II FEATURE EXTRACTION 9

Edge detection, Edge linking, corner detection, texture, binary shape analysis, boundary pattern analysis, circle and ellipse detection, Harris and Hessian Affine, Orientation Histogram, SIFT, SURF, HOG, Scale-Space Analysis- Image Pyramids and Gaussian derivative filters, Gabor Filters and DWT Shape from Texture, color, motion and edges.

UNIT III IMAGE SEGMENTATION AND SHAPE REPRESENTATION 9

Edge Based approaches to segmentation - Graph-Cut, Mean-Shift, MRFs, Texture Segmentation, Object detection, Lighting and Deformation - shadows, Lambertian, Harmonic images, deformable part models, fine-grained classification, Snakes and active contours, Fourier and wavelet descriptors, Multi-resolution analysis

UNIT IV MOTION ANALYSIS 9

Background Subtraction and Modeling, Optical computation, Optical Flow Stereo Vision, Motion estimation, KLT, Dynamic Stereo; Motion parameter estimation, Structure from motion, Object recognition - Shape correspondence and shape matching • Principal component analysis, Motion Tracking in Video

UNIT V APPLICATIONS OF COMPUTER VISION 9

Artificial Neural network for patter classification- Biological neural system, categories, Neural Network Structures, Supervised learning, Unsupervised learning, Gesture recognition, Motion estimation - Surveillance, In-Vehicle Vision Systems, object tracking, CBIR, CBVR, computational photography, Biometrics, CVaaS, Emotion AI

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Articulate the concepts of imaging systems.
- Study the image formation models and feature extraction for computer vision
- Identify the segmentation and motion detection and estimation techniques
- Develop small applications and detect the objects in various applications
- Apply various algorithms to analyze real world scene and provide information about the real world objects.

REFERENCES:

1. Richard Szeliski, Computer Vision: Algorithms and Applications, Springer-Verlag London Limited, 2011.
2. D. A. Forsyth, J. Ponce: Computer Vision: A Modern Approach, Pearson Education, 2003.
3. E. R. Davies “Computer and Machine Vision: Theory, Algorithms, Practicalities”, 4th Edition, Elsevier Inc,2012.
4. Richard Hartley and Andrew Zisserman, Multiple View Geometry in Computer Vision, Second Edition, Cambridge University Press, March 2004.

5. Marco Alexander Treiber, Optimization for Computer Vision: An Introduction to Core Concepts and Methods, Springer 2013.
6. Alan C. Bovik, Handbook of Image and Video Processing, ISBN- 978-0123885623, ELSEVIER, ACADEMIC PRESS, 2005.
7. K. Fukunaga, "Introduction to Statistical Pattern Recognition", 2nd Edition, Morgan Kaufmann, 1990.

WEBSITE REFERENCES:

1. https://www.youtube.com/watch?v=yetsJWgYh0o
2. https://www.youtube.com/watch?v=7xKhYfPel9w
3. https://www.youtube.com/watch?v=yxID4fgz1C0
4. https://www.analyticsinsight.net/top-applications-of-computer-vision-in-industrial-settings/
5. https://www.youtube.com/watch?v=Tm4C2ZFd3zE
6. https://www.youtube.com/watch?v=jRrs9OxLTYM
7. https://www.sciencedirect.com/topics/computer-science/motion-analysis
8. https://www.analyticsinsight.net/top-5-computer-vision-trends-that-will-rule-2021/

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	2	2	2
CO2	3	2	3	2	2	3
CO3	3	3	2	3	3	2
CO4	3	3	3	3	3	2
CO5	3	3	3	2	3	2
AVG	3	2.6	2.6	2.4	2.6	2.2

JAE5211	**ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

COURSE OBJECTIVES:

- Students will carry out a detailed analog circuit design with transistor characterization.
- At various stages of design, a typical state of art CAD VLSI tool will be used in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.
- To Identify, formulate, solve and implement problems in digital systems on application level using RTL design tools
- To Implement the design using FPGA/CPLD devices
- To use EDA tools like Cadence and Xilinx

LIST OF EXPERIMENTS:

1. Extraction of process parameters of CMOS process transistors
2. CMOS inverter design and performance analysis
3. Use spice to build a three stage and five stagering oscillator circuit and compare its frequencies.
4. Use FFT and verify the amplitude and frequency components in the spectrum.
5. Single stage amplifier design and performance analysis.
6. Three OPAMP Instrumentation Amplifier.
7. Use Layout editor.
8. Design a differential amplifier with resistive load using transistors from CMOS process library.
9. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF
10. Verilog implementation of 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
11. Analysis of leakage current during reduction in CMOS SRAM cell

TOTAL: 60 PERIODS

COURSE OUTCOMES:

- Design digital and analog Circuit using CMOS given a design specification.
- Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances
- Use EDA tools like Cadence, Mentor Graphics or other open source software tools like LT Spice.
- Design layout for various digital integrated circuits.
- Design static and dynamic digital CMOS circuits.

LAB REQUIREMENTS:

1. Xilinx - 5 nos
2. Cadence – 5 nos
3. PCs – 5 nos

WEBSITE REFERENCES:

1. https://vlsi-iitg.vlabs.ac.in/CMOS_theory.html
2. http://vlabs.iitb.ac.in/vlabsdev/vlab_bootcamp/bootcamp/electronerds/experiments/instrumentation-amplifier-pvg/procedure.html
3. https://www.eecg.utoronto.ca/~johns/ece334/labs/lab4
4. https://www.youtube.com/watch?v=oL8SKNxEaHs, CMOS Digital VLSI
5. https://www.youtube.com/watch?v=3p_tGqCu8Ds, Introduction to CMOS Analog VLSI

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO-1	3	3	2	3	3	1
CO-2	3	3	2	3	3	1
CO-3	3	3	3	3	3	1
CO-4	3	3	2	3	3	2
CO-5	3	3	2	3	3	2
AVG	3	3	2.2	3	3	1.4

JAE5241	MINI PROJECT	L	T	P	C
		0	0	4	2

COURSE OBJECTIVES

- To develop skills to formulate a technical project and prepare technical report of the project.
- To estimate the ability of the student in transforming the theoretical knowledge studied so far into a working model of an Electronics and Communication system.
- To teach use of new tools, algorithms and techniques required to carry out the projects.
- To give guidance on the various procedures for validation of the product and analyze the cost effectiveness.
- For enabling the students to gain experience in organization and implementation of a small project and thus acquire the necessary confidence to carry out main project in the final year.

COURSE GUIDELINES

- The students are required to search / gather the material / information on a specific a topic comprehend it and present via ppt, prototype model, video etc., to the panel for further discussion and approval.
- Each student works on the approved topic should make a hardware/software model which shall be a working model or simulated output. The progress of the project should be presented and get evaluated by a reviewer committee constituted by the head of the department.
- The student should prepare a comprehensive mini project report after completing the work to the satisfaction of the reviewer committee. The mini project work is evaluated based on oral presentation and the mini project report jointly by external and internal examiners constituted by the Head of the Department.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- Formulate a real world problem, identify the requirement and develop the design solutions.
- Express the technical ideas, strategies and methodologies.
- Utilize the new tools, algorithms, techniques that contribute to obtain the solution of the project.
- Test and validate through conformance of the developed prototype and analysis the cost effectiveness.
- Prepare report and present the oral demonstrations.

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	2
CO2	3	3	3	3	3	2
CO3	3	2	3	1	3	3
CO4	3	3	3	3	3	3
CO5	3	2	3	3	2	3
AVG	3	2.6	3	2.6	2.6	2.6

JAE5251	TERM PAPER WRITING AND SEMINAR	L	T	P	C
		0	0	2	1

COURSE OBJECTIVES:

- To revamp the knowledge gained in the semester and prepare the students to face interview both at the academic and the Industrial Sector
- To encourage the students to study about the recent developments in the field
- To prepare and present technical reports
- To encourage the students to use various teaching aids such as Power point presentation and Demonstrative models

METHOD OF EVALUATION:

TERM PAPER WRITING:

The students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

- Selecting a topic and an objective.
- Collecting the relevant bibliography (atleast 15 journal papers)
- Preparing a working outline.
- Studying the papers and understanding the author's contributions and critically analysing it.
- Linking the papers and preparing a draft of the paper.
- Preparing conclusions based on the reading of all the papers.
- Writing the Final Paper

SEMINAR:

Three periods are allotted for the technical seminar. During the seminar session each student is expected to prepare and present a technical topic for duration of 10 minutes.
Each student is expected to make presentation at least twice during the semester and the student is evaluated based on various parameters such as topic chosen, content delivery, communication skills and presentation. A faculty guide is allotted who shall guide and monitor the progress and attendance of all the students. Equal weightage is considered for the two seminar sessions for a total weightage of 50 marks.

The total mark awarded for the course shall be the sum of marks scored out of 50 each for the two components. Evaluation is purely internal.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Consolidate all the engineering concepts acquired in the course of study.
- Enrich their technical knowledge.
- Prepare and present technological developments.
- Communicate effectively the concepts related to the various topics.
- Face the interviews with confidence during the placement drives.

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	2
CO2	3	3	3	3	3	2
CO3	3	2	3	1	3	3
CO4	3	3	3	3	3	3
CO5	3	2	3	3	2	3
AVG	3	2.6	3	2.6	2.6	2.6

SEMESTER-3

JRM5301	RESEARCH METHODOLOGY AND IPR	L	T	P	C
		2	0	0	2

COURSE OBJECTIVES:

- To identify and prepare the research problem.
- To reexamine the literature and research ethics.
- To associate the research design in the report.
- To explore and integrate the Intellectual Property Rights in research.
- To be aware of patent procedure and penalties.

UNIT I RESEARCH PROBLEM FORMULATION 6

Meaning of research problem- Sources of research problem, characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem- Types of research-Research Approaches-Research Process-Approaches of investigation of solutions for research problem.

UNIT II LITERATURE REVIEW 6

Reviewing the literature- Procedure for reviewing the literature-Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III TECHNICALWRITING /PRESENTATION 6

Important Concepts Relating to Research Design-Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal.

UNIT IV INTELLECTUAL PROPERTY RIGHTS (IPR) 6

Need for Intellectual Property right – Nature, scope and importance of IPR- Types of Intellectual property – IPR in Technological research and innovation – National IPR Policy- objectives and achievements – Issues in India's IPR Regime.

UNIT V PATENTS 6

Core objectives – elements of patentability – Patent search – Registration procedure, specification – rights and duties of patentee, assignment and license, restoration of lapsed patents, infringement, remedies & penalties – procedure for grants of patents.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able,

- To investigate and formulate the research problem.
- To correlate the research analysis through review of literature.
- To prepare research report effectively.
- To apply IPR in Technological research and innovation.
- To be aware with the adequate knowledge on patent and rights.

TEXT BOOKS

1. Kothari, C.R., 2004, Research Methodology: Methods and Techniques. New Age International.
2. Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers,"Patent searching: tools & techniques", Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

REFERENCES

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners" 2010
2. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers
3. Robert P. Merges, Peter S. Menell and Mark A. Lemley, "Intellectual Property in New Technological Age", Aspen Publishers, 2016.
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

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2. https://gradcoach.com/what-is-research-methodology/
3. https://www.scribbr.com/category/methodology/
4. Cell for IPR Promotion and Management (http://cipam.gov.in/)
5. World Intellectual Property Organisation (https://www.wipo.int/about-ip/en/)
6. Office of the Controller General of Patents, Designs & Trademarks (http://www.ipindia.nic.in/)

CO-PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO-1	1	1	3	3	3	2
CO-2	1	3	3	3	2	2
CO-3	1	1	1	2	2	2
CO-4	3	2	3	2	1	1
CO-5	3	2	3	2	1	1

JAE5361	PROJECT WORK - PHASE - 1	L	T	P	C
		0	0	12	6

COURSE OBJECTIVES:

- To identify a specific problem for the present need of the society and collecting information related to the same through detailed literature survey.
- To develop the methodology to solve the identified problem.
- To design, analyze and simulate the chosen problem using the software package.
- To train the students in preparing project reports and to face reviews and viva-voce examination.

METHOD OF EVALUATION:

The students work on a topic approved by the Head of the Department under the guidance of a faculty member, prepare a comprehensive project report after completing the work to the satisfaction of the supervisor. The progress of the project is evaluated based on a minimum of three reviews. The review committee is constituted by the Head of the Department. The project work is evaluated based on oral presentation and the project report, jointly by external and internal examiners.

COURSE OUTCOMES:

On completion of the phase - 1 project work, the students will be able to

- Analyze and formulate the problem
- Identify the methodology needed to solve the problem.
- Identify the tools and techniques required to solve the problem.
- Work with team mates to acquire the required material needed to find solutions to the chosen problem.
- Effectively communicate the outcomes of the findings.

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	2	2
CO2	3	3	3	3	3	2
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	2	3
AVG	3	3	3	2.8	2.6	2.6

JAE5321	TECHNICAL SEMINAR	L	T	P	C
		0	0	2	1

COURSE OBJECTIVES:

- To revamp the knowledge gained in the semester and prepare the students to face interview both at the academic and the Industrial Sector
- To encourage the students to study about the developments in the field
- To prepare and present technical seminars
- To train the students in preparing project reports and to face reviews and viva-voce examination.

METHOD OF EVALUATION:

SEMINAR:

Three periods are allotted for the technical seminar. During the seminar session each student is expected to prepare and present a technical topic for duration of 10 minutes.
Each student is expected to make presentation at least twice during the semester and the student is evaluated based on various parameters such as topic chosen, content delivery, communication skills and presentation. A faculty guide is allotted who shall guide and monitor the progress and attendance of all the students. Equal weightage is considered for the two seminar sessions for a total weightage of 50 marks.

The total mark awarded for the course shall be the sum of marks scored out of 50 each for the two components. Evaluation is purely internal.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Consolidate all the engineering concepts acquired in the course of study.
- Enrich their technical knowledge.
- Prepare and present technological developments.
- Communicate effectively the concepts related to the various topics.
- Face the interviews with confidence during the placement drives.

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	2
CO2	3	3	3	3	3	2
CO3	3	2	3	1	3	3
CO4	3	3	3	3	3	3
CO5	3	2	3	3	2	3
AVG	3	2.6	3	2.6	2.6	2.6

JAE5461	PROJECT WORK - PHASE - 2	L	T	P	C
		0	0	24	12

COURSE OBJECTIVES:

- To develop the ability to solve a specific problem related to their subject expertise.
- To develop the methodology to solve the identified problem.
- To design, analyze and implement the chosen problem using the hardware components.
- To validate the simulation, hardware results with the theoretical results.
- To train the students in preparing project reports and to face reviews and viva-voce examination.

METHOD OF EVALUATION:

The students work on a topic approved by the Head of the Department under the guidance of a faculty member, prepare a comprehensive project report after completing the work to the satisfaction of the supervisor. The progress of the project is evaluated based on a minimum of three reviews. The review committee is constituted by the Head of the Department. The project work is evaluated based on oral presentation and the project report, jointly by external and internal examiners.

COURSE OUTCOMES:

On Completion of the project work, the student will be able to

- Apply the technical knowledge acquired for solving real world problems.
- Develop skills such as self learning, critical thinking, problem solving, project management and finance.
- Apply modern tools and techniques.
- Work with team mates and collectively work towards the success of the project.
- Communicate effectively to present the outcomes of the project both in written and oral forms.

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	2	2	2
CO2	3	3	3	3	3	2
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	2	3
AVG	3	3	3	2.8	2.6	2.6

PROFESSIONAL ELECTIVES – 1

SEMESTER I

JAE5001	SENSORS, ACTUATORS AND INTERFACE ELECTRONICS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand static and dynamic characteristics of measurement systems.
- To study various types of sensors.
- To study about self-generating sensors
- To study different types of actuators and their usage.
- To study State-of-the-art of digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

General concepts and terminology – measurement systems – sensor classification –general input-output configuration – methods of correction – performance characteristics: static characteristics - dynamic characteristics of measurement systems: zero-order - first-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS 9

Potentiometers:– resistive temperature detectors – magneto resistors – Light-dependent resistors – Reactance variation: Capacitive sensors: humidity sensor – Inductive sensor - linear variable differential transformers (LVDT) – Electromagnetic sensors: Magneto elastic sensors – hall effect sensors.

UNITIII SELF- GENERATING SENSORS 9

Thermoelectric sensors – piezoelectric sensors – pyroelectric sensors – photovoltaic sensors – electrochemical sensors – Signal conditioning for self-generating sensors: chopper and low-drift amplifiers – offset and drifts amplifiers – electrometer amplifiers – noise in amplifiers.

UNITIV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9

Relays – Solenoid drive – Stepper Motors – Voice-Coil actuators – Servo Motors – DC motors and motor control – 4-to-20 mA Drive – Hydraulic actuators – Pneumatic actuators – Variable transformers: synchros- resolvers - Inductosyn – resolver-to-digital and digital-to-resolver converters.

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSOR 9

Position encoders – optical encoder – variable frequency sensors – quartz digital thermometer – vibrating sensors: vibrating wire strain gages- vibrating cylinder sensors – Surface Acoustic Waves sensors – digital flow meters – magneto diodes and magneto transistors – photodiodes and phototransistors – CCD imaging sensors – ultrasonic sensors – fiber-optic sensors.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- Explain basics of measurement system
- Discuss about different types of sensors
- Discuss about Self-generating sensors
- Compare different types of Actuators
- Evaluate digital sensors and semiconductor device sensors

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1. Jacob Fraden, "Hand Book of Modern Sensors: physics, Designs and Applications", Third Edition, Springer, New York 2015.
2. Clarence W. de Silva Author. Sensors and Actuators: Engineering System Instrumentation, Second Edition , CRC Press ,2015.
3. Jon. S. Wilson, "Sensor Technology Hand Book", First Edition, Elsevier, Netherland 2011.
4. E.O.Doeblin, "Measurement System: Applications and Design", Fifth Edition McGraw Hill publications 2004.
5. Kevin James, "PC Interfacing and Data acquisition", First Edition ,Elsevier,2011.
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3. https://nptel.ac.in/content/storage2/courses/112104158/lecture36.pdf- Dr. Bihkh Bishakh Bh tt h Bhattacharya Professor, Department of Mechanical Engineering IIT Kanpur
4. https://nptel.ac.in/content/storage2/courses/112108092/module1/lec04.pdf G.K. Ananthasuresh Professor, Mechanical Engineering Indian Institute of Science Bangalore, 560012, India
5. https://nptel.ac.in/content/syllabus_pdf/108108147.pdf Prof Hardik J Pandya Department of Electrical & Electronic Engineering IISc Bangalore.

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5
CO1	3	3	2	1	2
CO2	3	3	2	1	2
CO3	3	3	2	1	2
CO4	3	3	2	1	2
CO5	3	3	2	1	2
AVG	3	3	2	1	2

JAE5002	ANALOG INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
- To analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To design and analyse feedback amplifiers and one stage op amps
- To design and analyse two stage opamps
- To design and use current mirrors and current sinks with MOS devices

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op-Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op-Amps, Low voltage gain boosting schemes.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis of two stage Op-amp, multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, PLL.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascade sink, current amplifiers,Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing, Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- Ability to design amplifiers to meet user specifications
- Ability to analyse the frequency and noise performance of amplifiers
- Ability to design and analyse feedback amplifiers and one stage op amps
- Ability to design and analyse two stage opamps
- Ability to design and use current mirrors and current sinks with MOS devices

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1. Gray, Hurst, Lewis, and Meyer: "Analysis and design of Analog Integrated Circuits", 4th Edition, John Wiley and Sons
2. Behzad Razavi, "Design of Analog CMOSIntegratedCircuits",TataMcGrawHill,2001
3. David A.Johns and Ken Marting, "Analog Integrated Circuit Design", Wiley 2002
4. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
5. Grebene, "BipolarandMOSAnalogIntegratedCircuitDesign",JohnWiley&sons,Inc.,2003.
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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	1	3	3	1
CO2	3	3	1	3	2	1
CO3	3	2	1	3	3	1
CO4	3	2	1	3	3	1
CO5	2	3	1	2	3	1
AVG	2.8	2.4	1	2.8	2.8	1

JAE5003	**MEMS BASED DEVICES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices by understanding the essential material properties
- To study various sensing and transduction technique and educate on the rudiments of Micro fabrication techniques
- To know about RF MEMS
- To study about optical MEMS
- To construct models using MEMS systems

UNIT I INTRODUCTION TO MEMS 9

Principles of Microsystems, Nano and Micro scale systems, devices and structures, Micro structures, Axial stress and strain, Shear stress and strain, Static bending of beams and thin plates, Mechanical vibration, Stiction issue, Scaling laws in miniaturization and Materials, MEMS Materials, Case Study: Active and Passive MEMS.

UNIT II ACTUATION MECHANISMS IN MEMS AND FABRICATION 9

Electrostatic Actuators-charge and voltage control, linearization methods, comb drive actuators, levitation, Piezoelectric, Thermal, Magnetic actuators, gap closers, rotary finger pull up, MEMS Fabrication-Bulk micromachining, Surface micromachining, Thin-film depositions, Packaging-Microsystems packaging, 3D packaging, Case Study: NEMS, System on Chip.

UNIT III RF MEMS 9

Introduction to RF MEMS, general concepts in high frequency effects, RF MEMS Switches - RF switch design, RF filters with MEMS, Tunable Capacitors and Inductors, RF MEMS resonators and their applications, Comparison of electrostatic and piezoelectric resonators, Case Study: Micro machined antennas, Microstrip antenna, Reconfigurable antennas, RF MEMS Smartuners.

UNIT IV MICRO OPTO ELECTRO MECHANICAL SYSTEM 9

Digital Micro mirror Device, Grating Light Valve, Optical switches, optical filters, arrayed waveguide grating, Electrostatic reflective light modulator, Torsion mirror Micro machined optical structures, Fiber-optic couplers, Refractive lenses, Diffractive lenses, Waveguide optical systems, MEMS deformable mirrors, Adaptive MOEMS, Case study: Grating Light Valve.

UNIT V MODELLING OF MEMS SYSTEMS 9

Circuit Modeling of MEMS: resonator equivalent circuits, thermal circuits, fluidic circuits, general filter topologies, insertion loss, shape factor, resonator and couplers, circuit modeling of coupled resonators, systematic micromechanical filter design procedure, Electro-statically actuated micro-mirror, design of optical filters, case studies: MEMS gyroscopes.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, students will be able to:

- Analyze the mechanical performance of micro systems.
- Understand the operational theory of common MEMS actuators and analyze different MEMS technologies.
- Develop ideas in the micro machined designs for the design of reconfigurable antennas.
- Analyze the engineering science and physics of MEMS devices at the micro scale in optics.
- Develop new ideas and applications for MEMS devices.

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2. Stephen D.Senturia, “Microsystem Design”, Kluar Publishers, 2001.
3. Nadim Maluf, “An Introduction to Micro electro mechanical Systems Engineering”, Artech House, 2000.
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5. N.P.Mahalik, “MEMS”,Tata McGraw Hill, 2007.
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3. https://www.coursera.org/lecture/sensor-manufacturing-process-control/2-mems-construction-0tHJV
4. https://engineering.purdue.edu/online/courses/fundamentals-mems
5. https://www.microwaves101.com

CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	1	1	1	1
CO2	3	3	2	2	2	1
CO3	2	2	3	2	2	1
CO4	2	2	3	2	3	2
CO5	3	2	2	3	3	2
AVG	2.4	2.2	2.2	2	2.2	1.4

JAE5004	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture
- To familiarize the high performance features in RISC architecture
- To introduce the basic features in Motorola microcontrollers.
- To enable the students to understand PIC Microcontroller

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set— Registers and Addressing modes–Memory hierarchy—Cache–Virtual memory and paging – Segmentation- pipelining – pipelinehazards – instruction level parallelism – reduced instruction set — RISC versus CISC- need for hybrid processor

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE– PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Branch predication – floating point unit-Operating Modes –Paging — Multitasking — Exception and Interrupts — Instruction set — addressing modes– Programming the Pentium processor- 8 bit CISC CPU using FPGA.

UNIT III HIGHPERFORMANCE RISCARCHITECTURE–ARM 9

Organization of CPU — Bus architecture –Memory management unit - ARM instruction set-Thumb Instruction set-addressing modes–Programming the ARM processor- Introduction to RISC-V architecture.

UNIT IV MSP430 16-BIT MICROCONTROLLER 9

The MSP430 Architecture- CPU Registers -Instruction Set, On-Chip Peripherals -MSP430 - Development Tools, ADC-PWM-UART-Timer Interrupts-System design using MSP430 Microcontroller-A study of Modern Mine Surveillance using MSP430.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture– Instruction set– interrupts- Timers- I2C Interfacing– UART A/D Converter – PWM and introduction to C-Compilers - Application of PIC in Industrial instrumentation devices

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- To understand the fundamentals of microprocessor architecture.
- To know and appreciate the high performance features in CISC architecture.
- To know and appreciate the high performance features in RISC architecture.
- To perceive the basic features in Motorola microcontrollers.
- To interpret and understand PIC Microcontroller

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2. James L. Antonakos , “ The Pentium Microprocessor „“ Pearson Education , 1997.
3. Steve Furber , „“ ARM System –On –Chip architecture “Addision Wesley , 2000.
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6. John H.Davis , “MSP 430 Micro controller basics”, Eelsevier, 2008.
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4. Dr.Santanu Chaudhury, IIT Delhi, PIC Peripherals On Chip, https://www.youtube.com/watch?v=z-jt2oUHICQ
5. https://nptel.ac.in/courses/108/105/108105102/

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	2	2	2	1
CO2	2	2	3	2	3	1
CO3	2	2	3	3	3	1
CO4	2	2	3	3	3	1
CO5	2	2	3	2	3	1
AVG	2	2	3	2	3	1

PROFESSIONAL ELECTIVES – 2

SEMESTER 2

JAE5005	WIRELESS ADHOC AND SENSOR NETWORKS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the basics of Ad-hoc and Sensor Networks.
- To learn various fundamental and emerging protocols of all layers.
- To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
- To understand the nature and applications of Ad-hoc and sensor networks.
- To understand various security practices and protocols of Ad-hoc and Sensor Networks.

UNIT I MAC AND TCP IN ADHOC NETWORKS 9

Fundamentals of WLANs, IEEE 802.11 Architecture, Self configuration and Auto configuration, Issues in Ad-Hoc Wireless Networks, MAC Protocols for Ad-Hoc Wireless Networks, Contention Based Protocols, TCP over Ad-Hoc networks, TCP protocol overview, Solutions for TCP over Ad-Hoc Networks. Case study: TCP and MANETs, iMANET.

UNIT II ROUTING IN ADHOC NETWORKS 9

Proactive and Reactive routing approaches, Hybrid Routing Approach, Topology based versus Position based Approaches, Principles and issues, Location services, DREAM, Quorums based location service, Grid, Forwarding strategies, Greedy packet forwarding, Restricted directional flooding, Case study: Hierarchical Routing, Issues and Challenges in providing QoS, OLSR.

UNIT III WIRELESS SENSOR NETWORKS DESIGN AND PROTOCOLS 9

Single node architecture, Sensor network design considerations, Energy Efficient Design principles, Physical Layer–Transceiver Design considerations, MAC Layer Protocols, Link Layer and Error Control issues, Routing Protocols, Mobile Nodes and Mobile Robots, Data Centric and Contention Based Networking, Case Study: Zigbee, LoRaWAN.

UNIT IV SENSOR MANAGEMENT 9

Transport Protocols and QOS, Congestion Control issues, Application Layer support, Sensor Management, Topology Control Protocols, Sensing Mode Selection Protocols, Time synchronization, Localization and positioning, Operating systems and Sensor Network programming, Case Study: Sensor Network Simulators, IoT.

UNIT V SECURITY IN ADHOC AND SENSOR NETWORKS 9

Security in Adhoc and Sensor networks, Key Distribution and Management, Software based Anti-tamper techniques, water marking techniques, Defense against routing attacks, Secure Adhoc routing protocols, Broadcast authentication WSN protocols, TESLA, Biba, Sensor Network Security Protocols, Case Study: SPINS, SDARP.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should be able to:

- Identify different issues in wireless adhoc and sensor networks.
- analyze protocols developed for adhoc and sensor networks.
- Identify and address the security threats in adhoc and sensor networks.
- Establish a Sensor network environment for different type of applications.
- Analyze security mechanisms developed for adhoc and sensor networks.

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1. Adrian Perrig, J.D.Tygar, "Secure Broadcast Communication: In Wired and Wireless Networks", Springer, 2006.
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CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	2	2	2	2
CO2	2	2	2	3	2	2
CO3	2	2	2	2	2	1
CO4	2	2	2	2	2	2
CO5	3	2	2	3	2	2
AVG	2.2	2.0	2.0	2.4	2.0	1.8

JAE5006	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits
- Understand the concept of testing and its approach
- Understand the algorithms in testing
- Understand the diagnosis of fault in a circuit under test

UNIT I TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan-based design – classical scan-based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs- Test Pattern Generator for QCA(MV Based)

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should be able to:

- Explain the concepts of Testing and fault modelling
- Explain the approaches for test generation
- Discuss the testing design
- Discuss test algorithms
- Explain fault diagnosis

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1. A.L.Crouch, “Design Test for Digital IC‟s and Embedded Core Systems”, Prentice Hall International, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3	1	1	1
CO2	2	2	3	3	3	3
CO3	2	2	3	2	1	1
CO4	2	2	3	1	3	3
CO5	2	2	3	2	1	1
AVG	2	1.8	3	1.8	1.8	1.8

JAE5007	**RF SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To learn the importance and issues in the design of RF
- To know the RF components and Impedance matching
- To learn the various power amplifiers
- To gain knowledge on designing the RF amplifiers
- To learn about RF Mixers, Oscillators

UNIT I RF ISSUES 9

Importance of RF design- Electromagnetic spectrum, RF behavior of passive components, chip components and circuit board considerations, scattering parameters, Properties of scattering parameter, smith chart and applications.

UNIT II RF COMPONENTS AND IMPEDANCE MATCHING 9

Passive IC components, RF diodes, BJT, RF FET'S, High electron mobility transistors, matching and biasing networks- impedance matching using discrete components, micro strip line matching networks, amplifier classes of operation and biasing networks.

UNIT III FEEDBACK SYSTEMSAND POWERAMPLIFIER 9

Stabilityoffeedbacksystems: Gainandphasemargin,Root-locustechniques,TimeandFrequency domain considerations, Compensation, General model— Class A, AB, B, C, D, Eand F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques.

UNIT IV RF AMPLIFIER DESIGNS 9

Characteristics, amplifier power relations, stability considerations, constant gain circles, constant VSWR circles, low noise circles broadband, high power and multistage amplifiers, Single ended and Differential LNA.

UNIT V MIXERS, OSCILLATORS AND APPLICATIONS 9

Mixer characteristics, Nonlinear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, Colpitts oscillators, Tuned Oscillators, Negative resistance oscillators, Phase detectors, Loop filters, DigitalFrequencysynthesizers, SWIPT.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should be able to:

- Explain the importance and issues in the design of RF
- Analyze the RF components and design Impedance matching networks
- Explain the various power amplifiers
- Analyze and design the RF amplifiers
- Design RF Mixers, Oscillators

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1. Reinhold Ludwig and Gene Bogdanov, "RF Circuit Design: Theory and Applications", Pearson Education Inc., 2011
2. Mathew M. Radmanesh, Radio Frequency & Microwave Electronics, Pearson Education Asia, Second Edition, 2002.
3. Joseph. J. Carr, Secrets of RF Circuit Design , McGraw Hill Publishers, Third Edition,2000.
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6. B.Razavi,"RFMicroelectronics",PearsonEducation,1997.
7. The Design Of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee, 2nd Edition (2006) (Publisher: Cambridge University Press).

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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	3	2	2	1
CO2	3	2	3	3	3	1
CO3	2	3	2	2	3	2
CO4	3	3	3	3	2	1
CO5	3	2	3	2	3	1
AVG	2.6	2.6	2.8	2.4	2.6	1.2

JAE5008	**VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations
- To understand the various VLSI architectures for digital signal processing.
- To understand the advantages of pipelining and parallel processing of IIR filters.
- To train the code composer studio IDE to develop and debug arithmetic architectures.
- To familiarize in synchronous and asynchronous pipelined bundled data and the protocol

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Graphical representation of signals, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power. Dependence of graph.

UNIT II ALGORITHMIC STRENGTH REDUCTION – I 9

Retiming – definitions, theorem and properties, Cutset retiming, Retiming IIR filters, Unfolding – Basic unfolding relation, properties of unfolding, Retiming for unfolding, Algorithmic strength reduction – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION -II 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV CODE COMPOSER STUDIO IDE 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save Array, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Ability to modify the existing or new DSP architectures and design efficient DSP architectures suitable for VLSI
- Apply retiming and algorithmic strength reduction technique optimize design parameters
- Apply high level algorithm transformation to optimize design parameters.
- Apply various Bit-level arithmetic architecture to design the multipliers
- Apply numeric strength reduction to reduce area and power in digital K3 filters

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1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. S.Y.Kuang, H.J. White house, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1995.
3. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.
4. John G. Proakis, Dimitris G. Manolakis, " Digital Signal Processing", Pearson, 2007.
5. Rabaey, "Digital Integrated Circuits: A Design Perspective", Pearson, 2016.

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2. https://onlinecourses.nptel.ac.in/noc19_ee70/preview
3. https://nptel.ac.in/courses/117/102/117102060/
4. http://people.ece.umn.edu/users/parhi/SLIDES/chap9.pdf
5. https://www.researchgate.net/publication/3604054_Systolic_architecture_for_the_VLSI_implementation_of_high-speedstaged_decodersquantizers

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	2
CO2	3	3	3	3	3	2
CO3	3	3	3	3	3	2
CO4	3	3	3	3	2	3
CO5	3	3	3	2	2	3
AVG	3	3	3	2.8	2.6	2.4

PROFESSIONAL ELECTIVES – 3

SEMESTER II

JAE5009	INTERNET OF THINGS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols and various services provided
- To build a small low cost embedded system using Raspberry Pi.
- To apply the concept of Internet of Things in the real world scenario and understand the basics of electronic circuit assembly
- To get an idea of some application area where IoT can be applied.

UNIT I INTRODUCTION TO INTERNET OF THINGS 9

Internet of Things – Evolution of IoT, Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

UNIT II ARCHITECTURE OF IoT 9

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model- Domain model - information model - functional model - communication model - IoT reference architecture, 5G in IoT Middleware

UNIT III IoT PROTOCOLS & SECURITY CONSIDERATIONS 9

Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – 6LowPAN - CoAP – Security in deployment of IoT, Security Challenges in 5G-Based IoT Middleware Systems

UNIT IV BUILDING IoT WITH RASPBERRY PI & ARDUINO 9

Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino.

UNIT V APPLICATIONS AND CASE STUDIES 9

Home automations - Smart cities, Smart cities - Environment – Energy – Retail – Logistics – Agriculture – Industry - Health and life style – Case study - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT -Amazon Web Services for IoT.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Articulate the main concepts, key technologies, strength and limitations of IoT.
- Identify the architecture, infrastructure models of IoT.
- Analyze various protocols and the core issues of IoT such as security, privacy and interoperability
- Design a portable IoT using Raspberry Pi
- Deploy an IoT application and connect to the cloud and analyze applications of IoT in real time scenario

REFERENCES:

1. Arshdeep Bahga, Vijay Madisetti, “Internet of Things – A hands-on approach”, Universities Press, 2015.
2. DieterUckelmann, MarkHarrison, Florian Michahelles, “Architecting the Internet of Things”,Springer-Verlag Berlin Heidelberg, 2011.
3. Honbo Zhou, “Internet of Things in the cloud: A middleware perspective”, CRC press2012.
4. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-onApproach)”, VPT, 1st Edition, 2014.
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- https://www.youtube.com/watch?v=JeZeGJ-MfxA
- https://iotdunia.com/difference-iot-m2m-communication/ IOT VS M2M
- https://docplayer.net/9841295-Architecting-the-internet-of-things.html
- https://www.codemag.com/Article/1607071/Introduction-to-IoT-Using-the-Raspberry-Pi
- https://www.elprocus.com/building-the-internet-of-things-using-raspberry-pi/
- https://docplayer.net/9841295-Architecting-the-internet-of-things.html

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	2
CO2	3	3	3	3	3	2
CO3	3	3	3	3	2	2
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3
AVG	3	3	3	2.6	2.4	2.4

JAE5010	NANOMATERIALS AND NANOTECHNOLOGY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To learn about the overview of Nano electronics.
- To study the basic components of electronic systems.
- To learn about sensor fabrication and applications.
- To study about the nanomaterials used in Energy applications.
- To enhance our knowledge on the nanomaterials employed for Environmental remediation

UNIT I OVERVIEW OF NANO-ELECTRONICS 9

Nano-scale electronics; Foundation of nano-electronics – low dimension transport, quantum confinement, Coulomb blockade and quantum dot; Ballistic transport and Quantum interferences; Landauer formula, quantization of conductance, example of Quantum point contact - nanophotonics.

UNIT II TWO-TERMINAL JUNCTION TRANSISTORS 9

Basic CMOS process flow; MOS scaling theory; Issues in scaling MOS transistors; Requirements for non-classical MOS transistor; PMOS versus NMOS; Design and construction of MOS capacitor; Integration issues of high-k MOS – interface states, bulk charge, band offset, stability, reliability; MOS transistor and capacitor characteristics.

UNIT III SENSORS AND ACTUATOR CHARACTERISTICS 9

Basics: types and working principles of sensors and actuators; Characteristic features: Range, Resolution, Sensitivity, Error, Repeatability, Linearity and Accuracy, Impedance, Nonlinearities, Static and Coulomb Friction, Eccentricity, Backlash, Saturation, Dead-band, System Response, Frequency Response.

UNIT IV NANOMATERIALS IN FUEL CELL AND STORAGE TECHNOLOGY 9

Micro-fuel cell technologies, integration and performance for micro-fuel cell systems - thin film and microfabrication methods - design methodologies - micro-fuel cell power sources - Supercapacitors - Applications of nano in IC chips

UNIT V EMERGING TECHNOLOGIES FOR ENVIRONMENTAL REMEDIATION 9

Use of nanoparticles for environmental remediation and water treatment- Role of dendrimer single enzyme-nanoparticle and metalloprotein- Gene cloning-Case studies on Nanomedicine.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- Understandthebasicsciencebehindthedesignandfabricationofnanoscalesystems.
- Gain knowledge in basics of nano electronics.
- Gather idea about materials and techniques used for sensor components.
- Know about the nanomaterials used in Energy applications.
- Enhance knowledge on the nanomaterials employed for Environmental remediation.

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1. K.E. Drexler, “Nano systems”, Wiley, 1992.
2. W. Ranier, “Nano Electronics and Information Technology”, Wiley, 2003.
3. Vielstich. Wiley," Handbook of fuel cells: Fuel cell technology and applications", CRC Press, 2003.
4. M.C. Petty, “Introduction to Molecular Electronics”,1995.
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2. Prof. A.K. Ganguli, Department of Nanotechnology, IIT Delhi, "Nano structured materials", https://www.youtube.com/watch?v=ebO38bbq0_4
3. Dr. Sunita Satyapal, Director of the Energy Department's Fuel Cell Technologies, https://www.youtube.com/watch?v=41Nb6juV6MI
4. Prof. Emanuel Peled,Tel Aviv University, https://www.youtube.com/watch?v=esjH3vpsfHs

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	2	2	2	1
CO2	2	2	3	2	3	1
CO3	2	2	3	3	3	1
CO4	2	2	3	3	3	1
CO5	1	2	2	2	3	1
AVG	2	2	3	2	3	1

JAE5011	EMI AND EMC IN SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the concepts related to Electromagnetic interference in PCBs.
- To learn various EMI coupling principles.
- To indulge knowledge on EMI control techniques and design procedures to make EMI compatible PCBs
- To learn electromagnetic compatibility issues with regard to the design of PCBS
- To learn, EMI standards and measurements in the design of PCBs

UNITI EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI,ESD; Radiation Hazards. Methods of eliminating interference, EMC Engineering Application.

UNITII EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling; Commonmode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, crosstalk; Field to cable coupling; Power mains and Power supply coupling, Switching noise and Decoupling in digital circuits.

UNITIII EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control, Lighting Protection.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations, Electrostatic discharge.

UNITV EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer, EMI test wave simulator; Need for standards, Civilian standards-CISPR, FCC, IEC, EN,ANSI;Militarystandards-MIL461E/462.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to:

- Gain enough knowledge to understand the concept of EMI/EMC related to product design & development.
- To analyze the different EM coupling principles and its impact on performance of electronic system.
- Analyze electromagnetic interference, highlighting the concepts of both susceptibility and immunity
- Interpret various EM compatibility issues with regard to the design of PCB sand ways to improve the overall system performance
- To obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries

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1. C.R.Paul, ”Introduction to Electromagnetic Compatibility”, John WileyandSons,Inc,1992.
2. HenryW.Ott., ”Noise Reduction Techniques in Electronic Systems”, AWiley Inter Science Publications, John Wiley and Sons, Newyork,1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house, Norwood,3rdEdition,1986.
4. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork,1996.
5. Don R.J. White Consultant Incorporate, “Handbook of EMI/EMC”, Vol I-V, 1988.
6. Dr Kenneth L Kaiser , “ The Electromagnetic Compatibility Handbook”, CRC Press 2005.
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4. https://www.youtube.com/watch?v=cWo_sVDTszY&list=PL5kBRBfvqzbXCQXRcChr9-kFpGy9r7VZ9
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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	3	2
CO2	3	2	2	3	2	1
CO3	3	3	3	3	2	1
CO4	3	3	2	2	2	1
CO5	2	3	2	3	3	1
AVG	2.8	2.8	2.2	2.6	2.4	1.2

JAE5012	PATTERN RECOGNITION	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To study the fundamental of pattern classifier.
- To know about various clustering concepts.
- To originate the various structural pattern recognition and feature extraction.
- To familiarize the role of Hidden Marko model and SVM in pattern recognition.
- To explore recent advances in pattern recognition.

UNIT I PATTERN CLASSIFIER 9

Overview of Pattern recognition – Discriminant functions – Supervised learning –Parametric estimation– Maximum Likelihood Estimation– Bayesian parameter Estimation- Problems with Bayes approach – Pattern classification by distance functions - Minimum distance pattern classifier.

UNIT II CLUSTERING 9

Clustering for unsupervised learning and classification – Clustering concept: K Means algorithm - C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION 9

Principle component analysis – Independent component analysis – Linear discriminant analysis – Feature selection: through functional approximation - heuristic approach – Elements of formal grammars – Syntactic description – Stochastic grammars –Structural Representation.

UNIT IV HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE 9

State Machines – Hidden Markov Models -Training – Classification – Support vector Machine - feature selection- Real Life applications of SVM -Introduction to deep learning.

UNITV RECENT ADVANCES 9

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Random Forest Classifier - Case Study using Fuzzy Pattern Classifier – Case Study of multiclass classification using deep learning.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the student will be able to:

- Classify the data and identify the patterns.
- Analyze clustered patterns.
- Utilize the given data set to extract and select features for Pattern recognition.
- Explain Markov models and support vector machine.
- Discuss on recent advances in pattern recognition

REFERENCES:

1. R.O.Duda, P.E.Hartand D.G.Stork, "Pattern Classification",JohnWiley,2001
2. C.M.Bishop, "Pattern Recognition and Machine Learning",Springer,2006.
3. AndrewWebb," Stastical Pattern Recognition", Arnold publishers,London,1999
4. M.Narasimha Murthy and V.Susheela Devi, "Pattern Recognition", Springer 2011.
5. Menahem Friedman , Abraham Kandel, "Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches", World Scientific publishing Co.Ltd,2000.
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4. https://www.youtube.com/watch?v=Z66_2_VG_k8, Introduction to Statistical Pattern Recognition
5. https://www.youtube.com/watch?v=mfePdDh9t6Q, Principles of Pattern Recognition I (Introduction and Uses)

CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	1	2	2
CO2	3	2	2	1	2	2
CO3	3	2	2	1	2	2
CO4	3	2	2	1	2	2
CO5	3	2	2	1	2	2
AVG	3	2	2	1	2	2

PROFESSIONAL ELECTIVES – 4

SEMESTER III

JAE5013	VOICE AND DATA NETWORKS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To provide knowledge of voice and data networks fundamentals
- To study various queuing models and scheduling mechanisms
- To know about various data link layer protocols and its design
- To study about network and transport layer protocols and algorithms
- To model various security algorithms and application layer protocols

UNIT I INTRODUCTION TO VOICE AND DATA NETWORKS 9

Network Design Issues, Network Performance Issues, Network Terminology, centralized and distributed approaches for networks design, Issues in design of voice and data networks. Layered and Layerless Communication, Cross layer design of Networks, Voice Networks and Switching techniques, Case Study: Statistical Multiplexing, VoLTE.

UNIT II QUEUING AND SCHEDULING MECHANISMS 9

Queuing Models of Networks, Traffic Models, Little's Theorem, Markov chains, M/M/1 Queuing System, M/M/m, M/M/∞, M/M/m/m andother Markov systems, Multiple Access Protocols, Aloha System, Carrier Sensing mechanism. Case Study: Scheduling Algorithms, Stochastic Network Calculus.

UNIT III DATA LINK LAYER DESIGN AND ITS PROTOCOLS 9

Data Networks and their design, Link layer design- Link adaptation, Link Layer Protocols, Retransmission Mechanisms-Stop and Wait ARQ, Hybrid ARQ, GoBackN ARQ, Selective Repeat protocols and their analysis, Case Study: Wired and Wireless LAN technologies, CAN Protocol.

UNIT IV NETWORK AND TRANSPORT LAYER 9

Inter-networking, Bridging, Global Internet, IP protocol and addressing, Sub netting, Classless Inter domain Routing, IP address lookup, Routing in Internet. End to End Protocols, TCPand UDP, Congestion control and avoidance, Additive Increase/MultiplicativeDecrease, SlowStart, FastRetransmit/Fast Recovery mechanisms.

Case Study: QoS in Networks, MPTCP, RUDP.

UNIT V NETWORK SECURITY AND APPLICATIONS 9

Security-Cryptography, Key Predistribution, Authentication Protocols, Pretty Good Privacy, Secure Shell, TLS, SSL, HTTPS, IP Security, Wireless Security-WPA1 and WPA2, Firewalls, Traditional Applications- Electronic Mail, HTTP, Web Services, Multimedia Applications-SDP, SIP, H.323, Infrastructure Services-DNS, SNMP. Case Study: Overlay Networks.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, students will be able to:

- Analyze about voice and data networks fundamentals
- Analyze the queuing models and scheduling mechanisms
- Familiarize protocols, algorithms and trade-offs of data link layer
- Understand the Routing and transport layer mechanisms
- Design various security algorithms and application layer protocols

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CO-PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	1
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CO5	3	3	3	3	2	1
AVG	3	2.8	3	3	2	1

JAE5014	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To learn about concepts of neural network and hyper planes.
- To understand the main rules based on Fuzzy logic and Neuro Fuzzy systems
- To study about evolutionary computation systems and Genetic algorithm.
- To gain knowledge of algorithms inspired by nature such as ant colony optimization.
- To explore Particle swarm optimization and foraging optimization in solving problems in the real world.

UNIT I NEURAL NETWORKS 9

Neural Networks: Back Propagation Network - generalized delta rule– Radial Basis Function Network – interpolation and approximation RBFNS – comparison between RBFN and BPN – Support Vector Machines: Optimal hyperplane for linearly separable patterns- optimal hyperplane for nonlinearly separable patterns – Inverse Modeling.

UNIT II FUZZY LOGIC SYSTEMS 9

Fuzzy Logic System: Basic of fuzzy logic theory - crisp and fuzzy sets - Basic set operation like union - interaction - complement - T-norm - T-conorm - composition of fuzzy relations- fuzzy if-then rules - fuzzy reasoning – Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System(ANFIS) - ANFIS architecture - Hybrid Learning Approach: MANFIS – CANFIS

UNIT III EVOLUTIONARY COMPUTATION & GENETIC ALGORITHMS 9

Evolutionary Computation (EC) - Features of EC - Classification of EC - Advantages –Applications – Genetic Algorithms: Introduction-Biological Background -Operators in GA- GA Algorithm- Binary Classification of GA–Applications.

UNIT IV ANT COLONY OPTIMIZATION 9

Introduction: From real to artificial ants - Theoretical considerations – Convergence proofs– ACO Algorithm– ACO and model based search–Application principles of ACO.

UNIT V PARTICLE SWARM OPTIMIZATION 9

Introduction: Principles of bird flocking and fish schooling –Evolution of PSO - Operating principles - PSO Algorithm – Neighborhood Topologies – Convergence criteria –Applications of PSO, Honey Bee Social Foraging Algorithms -ABC algorithm.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Design and train neural networks with different rules
- Devise fuzzy logic rules
- Implement genetic algorithms
- Implement ANT colony optimization technique for various problems
- Use PSO technique

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1. Wolfgang Ertel, "Introduction to Artificial intelligence", Springer, 2nd Edition, 2017
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4. Christopher M. Bishop,"Neural Networks for Pattern Recognition", Oxford University Press,1995
5. H.Zimmermann,"Fuzzy Set Theory and its Applications", Springer Science + Business Media New York,4th edition,2001.
6. David E.Goldberg,"Genetic Algorithms in search, Optimization & Machine Learning" , PearsonEducation,2006
7. Marco Dorigo and Thomas Stutzle, "Ant Colony optimization", Prentice Hall of India, NewDelhi,2004.
8. N P Padhy,"Artificial Intelligence and Intelligent Systems", Oxford University Press, 2005.
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2. https://nptel.ac.in/courses/117/108/117108048/ Pattern Recognition by Prof. P.S. Sastry, Department of Electronics & Communication Engineering, IISc Bangalore
3. https://www.youtube.com/watch?v=9iaQg1vp4wE- Pattern Recognition by Prof. P.S. Sastry, Department of Electronics & Communication Engineering, IISc Bangalore

CO -PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	1	2	1
CO2	3	2	3	1	2	1
CO3	3	2	3	1	2	1
CO4	3	2	3	1	2	1
CO5	3	2	3	1	2	1
AVG	3	2	3	1	2	1

JAE5015	**DSP INTEGRATED CIRCUITS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the fundamentals of DSP systems and ICs design.
- To learn single and multirate digital filter concepts and structures.
- To study the architecture of general purpose digital signal processors.
- To introduce various processing elements used in DSP IC design.
- To gain knowledge about synthesizing DSP architecture using VLSI technique

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Sampling of analog signals – Signal processing systems: Frequency response – Transfer functions. DFT- FFT – Discrete Cosine Transform – Image coding -Standard Digital Signal Processors – Application specific ICs for DSP – DSP system design – Integrated circuit design.

UNIT II DIGITAL FILTER STRUCTURES AND MULTIRATE SYSTEMS 9

FIR filter structures – IIR filters: Specifications- Filter Structures - Mapping of analog transfer functions- - Mapping of analog filter structures – Multirate systems: Interpolation with an integer factor L- Decimation with an integer factor M - Sampling rate change with a ratio L/M - Multirate filter bank application.

UNIT III DSP ARCHITECTURES 9

DSP system architectures: Standard DSP architecture – Harvard and Modified Harvard architecture – TMS320C54x and TMS320C6x architecture – Multiprocessors and multi-computers – MessageBased Architectures– Systolic and Wave front arrays – Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES AND IC DESIGN 9

Mapping of DSP algorithms on to hardware- Isomorphic Mapping of SFGs -Implementation based on complex Processing Elements - Shared memory architecture with Bitserial PEs-Layout of VLSI circuits – Layout Styles – Design of large DSP systems as case studies: FFT processor – DCT processor –Interpolator.

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS 9

Conventional number system- Redundant Number system- Residue Number System- Bit-parallel and Bit-Serial arithmetic - Fixed Coefficient Multipliers - Bit-Serial Squarer - Digit Serial arithmetic – CORDIC Algorithm – Distributed Arithmetic - Basic shift accumulator – Reducing the memory size – Complex multipliers – Improved shift accumulator.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able

- To analyze fundamental signal processing algorithms and systems.
- To explain digital filter concepts, structures and Multi rate systems.
- To elaborate the architecture of general purpose digital signal processors.
- To design DSP systems using VLSI design
- To elucidate the working concepts of various Processing elements in DSP

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6. B.Venkatramani, M.Bhaskar, "Digital Signal Processors",Tata McGraw-Hill,2002.
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4. https://pptsearch365.com/pg-course-dsp-integrated-circuits-lecture-notes-in-ppt.html
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CO -PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	2	2	2	1
CO2	2	2	3	3	3	1
CO3	2	1	3	2	2	1
CO4	2	2	3	3	3	1
CO5	2	1	3	2	3	1
AVG	2	1	3	2	3	1

JAE5016	ROBOTICS AND INTELLIGENT SYSTEMS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the basic concepts in robotics.
- To expose the various design aspects in robot grippers.
- Tolearn various drives andcontrol systems.
- To impart knowledge on machine vision systems.
- To apply robot based concepts for automation

UNIT I INTRODUCTION 9

Introduction to robotics, three laws, DOF, Misunderstood devices, Elements of Robotic Systems, Robot anatomy, Classification, Associated parameters-resolution, accuracy, repeatability, dexterity, compliance, RCC device. Automation-Concept, Need,Automation in Production System, Principles and Strategies of Automation, Basic Elements ofan Automated System, Advanced Automation Functions, Levels of Automations, introduction toautomationproductivity.

UNIT II ROBOT GRIPPERS 9

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system.Sensors for Robots-Characteristics of sensing devices, Selections of sensors, Classificationand applications of sensors. Types of Sensors, Need for sensors and vision system in theworkingandcontrol ofarobot.

UNIT III DRIVES AND CONTROL SYSTEMS 9

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems-Types of Controllers, Introduction to closed loop control, Control Technologies in Automation-Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Control System Components-Sensors, Actuators, Mobile Robots: Position, and Orientation

UNIT IV MACHINE VISION SYSTEM 9

Vision System Devices, Robot Programming- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages, Features of type and development of languages for recent robot systems, Flying and Swimming Robots.

UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9

Introduction to system Modeling, Building Mathematical Model of a manufacturing Plant, Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy decision and control, Application of robots for automation, Artificial Intelligence- Introduction to AI, AI techniques, Need and application of AI, Tele-robotics, Micro & Nanorobots, Cognitive robotics.

TOTAL:45PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Implement simple concepts associated with Robotics and Automation
- Use various Robotic sub-systems
- Use kinematics and dynamics to design exact working pattern of robots
- Implement computer vision algorithms for robots
- Know and understand associated recent updates in Robotics

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3. ShimonY. Nof, "Handbook of Industrial Robotics", John Wiley Co, 2001.
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3. https://nptel.ac.in/courses/112/107/112107289/ Prof. N. Sukavanam Department of Mathematics IIT Roorkee, Prof.M. Felix Orlando, Department of Electrical Engineering, IIT-Roorkee.
4. https://nptel.ac.in/courses/106/105/106105077/Prof. Anupam Basu, Department of Computer Science and Engineering, IIT Kharagpur.

CO-PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	2	2	1	1
CO2	3	3	1	3	3	1
CO3	3	2	2	3	2	1
CO4	2	3	3	2	3	1
CO5	3	3	1	3	2	1
AVG	2.6	2.6	1.8	2.6	2.2	1

PROFESSIONAL ELECTIVES – 5

SEMESTER III

JAE5017	COGNITIVE NETWORKS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To gain knowledge on the fundamental concepts of cognitive radio networks.
- To understand the techniques for spectrum holes detection that cognitive radio takes advantages in order to exploit it.
- To learn technologies to allow an efficient use of TVWS for radio communications based on two spectrum sharing business models / policies.
- To know the fundamental issues regarding dynamic spectrum access, the radio-resource management and trading, as well as a number of optimization techniques for better spectrum exploitation.
- To know the research challenges in cognitive radio

UNIT I INTRODUCTION TO COGNITIVE RADIOS 9

Digital dividend, cognitive radio (CR) architecture, functions of cognitive radio, dynamic spectrum access (DSA), components of cognitive radio, spectrum sensing, spectrum analysis and decision, potential applications of cognitive radio.

UNIT II SPECTRUM SENSING 9

Spectrum sensing, detection of spectrum holes (TVWS), collaborativesensing, geo-location database Optimization Techniques of Dynamic Spectrum Allocation: Linear programming, convex programming, non-linear programming, integer programming, dynamic programming, stochastic programming.

UNIT III DYNAMIC SPECTRUM ACCESS AND MANAGEMENT 9

Spectrumbroker, cognitive radio architectures, centralized dynamic spectrum access, distributed dynamic spectrum access, learning algorithms and protocols.

UNIT IV SPECTRUM TRADING 9

Introduction to spectrum trading, classification of spectrum trading, radio resource pricing, brief discussion on economics theories in DSA (utility, auction theory), classification of auctions (single auctions, double auctions, concurrent, sequential).

UNIT V RESEARCH CHALLENGES IN COGNITIVE RADIO 9

Network layer and transport layer issues, cross-layerdesignforcognitiveradio networks, Effects of Trust Management –Security properties in CRN –Route Disruption attacks –Jamming attacks –PU Emulation attacks, CR based IoT.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, students will be able to:

- Describe the fundamental concepts of cognitive radio networks.
- Develop the cognitive radio, as well as techniques for spectrum holes detection that cognitive radio takes advantages in order to exploit it.
- Explain technologies to allow an efficient use of TVWS for radio communications based on two spectrum sharing business models / policies.
- Analyze fundamental issues regarding dynamic spectrum access, the radio-resource management and trading, as well as a number of optimization techniques for better spectrum exploitation.
- Analyze the research challenges in cognitive radio.

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1. Kwang-Cheng Chen, Ramjee Prasad, "Cognitive radio networks", John Wiley &Sons Ltd.,2009.
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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	3	2	2	1
CO2	3	2	3	3	3	1
CO3	2	3	2	2	3	2
CO4	3	3	3	3	2	1
CO5	3	2	3	2	3	1
AVG	2.6	2.6	2.8	2.4	2.6	1.2

JAE5018	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To learn the basic structure and operations of a computer and the importance of scalable architectures
- To learn the difference between pipeline and parallel processing concepts
- To study Memory Architectures, Memory Technology and Optimization.
- To know about the importance of multiprocessor
- To understand the need for multi-core processors, and its architecture.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multi-vector and SIMD architectures–Multithreaded architectures–Stanford Dash multiprocessor–KSR1-Data-flow architectures –Performance Measures

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Pipelining processors -Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation -Multiple Issue Processors-Performance and Efficiency in Advanced Multiple Issue Processors, Case study: Dynamic Scheduling in Intel Core i7 and ARM Cortex-A8.

UNIT III MEMORY HIERARCHY DESIGN 9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance–Memory Protection and Virtual Memory-Design of Memory Hierarchies, Case Study: Memory Hierarchies in Intel Core i7 and ARM Cortex-A8.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures–Cache coherence issues–Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks –Buses, cross brand multi-stage switches. Multiprocessor operating system, parallel algorithms for multiprocessors.

UNIT V MULTI-CORE ARCHITECTURE 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUNCMP architecture – IBM cell architecture – hparchitecture, Application of Multi-core and GPU Architectures on Signal Processing.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, students will be able to:

- Obtain broad knowledge in basic structure and operations of a computerand the importance of scalable architectures.
- Analyze the difference between pipeline and parallel processing concepts.
- Analyse the Memory Architectures, Memory Technology and Optimization.
- Describe the importance of multiprocessor.
- Describe multicore architectures and identify their characteristics and challenges.

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CO - PO MAPPING

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	3	2	2	2
CO2	3	2	3	3	3	2
CO3	3	2	3	3	3	2
CO4	3	2	3	3	3	2
CO5	3	2	3	3	3	2
AVG	**2.8**	**2**	**3**	**2.8**	**2.8**	**2**

JAE5019	DIGITAL SYSTEM TESTING AND TESTABLE DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To design of an efficient testable circuit and optimal test vectors to detect all possible detectable faults in a digital system.
- To analyze the fault analysis, test generation and design for testability for digital integrated circuits and systems are discussed in depth.
- To gain knowledge on the basics of digital testing techniques.
- To introduce the concept development of automatic test pattern generation of digital circuits.
- To discuss the fundamentals of design of testability.

UNIT 1 FUNDAMENTALS OF DIGITAL TESTING 9

Design and Test, Test Concerns, HDLs in Digital System Test, ATE Architecture and Instrumentation - Using Verilog in Design, Using Verilog in Test, Basic Structures of Verilog, Combinational Circuits, Sequential Circuits.

UNIT II FAULT MODELING & SIMULATION 9

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance – Single stuck fault model and multiple stuck fault model- Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation- Fault Simulation Techniques- Serial, Parallel and Deductive

UNIT III TEST GENERATION 9

Test Generation Basics, Controllability and Observability, Random Test Generation - Deterministic Test Generation Methods, Sequential Circuit Test Generation, Test Data Compaction - Making Circuits Testable, Testability Insertion, VPN.

UNIT IV DESIGN OF TESTABILITY 9

Full Scan DFT Technique, Scan Architectures and RT Level Scan Design - Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, RT Level Boundary Scan and Boundary Scan Description Language - Logic Built-in Self-test: BIST Basics.

UNIT V TESTABLE DESIGN 9

Test Pattern Generation, Output Response Analysis, BIST Architectures, RT Level BIST Design Test Data Compression, Compression Methods and Decompression Methods Memory Testing, Memory Structure, Memory Fault Model, Functional Test Procedures and MBIST Methods, PLA Testing.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, students will be able to:

- Analyze the fundamentals of digital system testing and its basics.
- Analyze the various fault models and fault simulation techniques.
- Develop the models and test generation algorithms
- Interpret different testability methods
- Analyze the different methods of test generation and compression

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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	2	3
CO2	3	2	2	3	3	3
CO3	3	2	3	3	3	3
CO4	3	2	3	3	3	3
CO5	3	2	3	3	3	3
AVG	**3**	**2**	**2.6**	**3**	**3**	**3**

JAE5020	COMPUTER NETWORK SECURITY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the concepts of security attacks, standards and challenges and its need.
- To be familiar with the various human security threats, ways in which users can aid security
- To determine appropriate mechanisms for protecting networked systems by applying various cryptographic techniques.
- To learn the function of a firewall, and how it keeps a computer secure and safe from viruses.
- To learn about Security in Wireless Network and Devices and sensor networks

UNIT I INTRODUCTION TO COMPUTER NETWORK SECURITY 9

Need for Security-Security Attacks - standards- challenges, sources of security threats, threat motives, management and correlation - security threat awareness-System security policy, Building, specification, Threat Identification and analysis Services and Mechanisms.

.

UNIT II ORGANIZATIONAL SECURITY 9

Password selection, Piggybacking, Shoulder surfing, Dumpster diving, Installing unauthorized software/hardware, Access by non-employees. People as Security Tool: Security awareness, and Individual user responsibilities.

UNIT III CRYPTOGRAPHY 9

Cryptography Defination, Symmetric Encryption, public key encryption, enhancing security and Key management; Public key Infrastructure, hash function, HMAC and digital signatures- Lenstra-Verheul Model for Key Sizes, Internet Security Protocols.

UNIT IV SYSTEM SECURITY 9

System Intrusion Detection and Prevention: Intrusion detection mechanism, types, Response, challenges to intrusion detection systems and implementations, Intrusion prevention systems

Firewall, Virus and Content Filtering: Firewall Characteristics, Types, Basing Location and Configurations-Scanning, Filtering and blocking - Introduction to Computer and Network Forensics.

UNIT V WEB SECURITY 9

Security in Wireless Network and Devices: WLAN security concerns and best practices for WIFI security. security in sensor networks: Challenges, vulnerabilities and attacks, security mechanisms and best practices for sensors.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Identify the threat awareness, security policy, Identification and analysis Services and Mechanisms.
- Provide Security awareness, and Individual user responsibilities
- Identify solution for each functionality at each layer
- Identify solution Various system security applications
- Identify solution Various network security applications

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CO - PO MAPPING

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	3	1
CO2	3	2	3	3	3	1
CO3	3	3	3	3	3	1
CO4	3	3	3	3	3	1
CO5	3	3	3	3	3	1
AVG	3	2.6	3	3	3	1

OPEN ELECTIVE-1

SEMESTER III

JAE9001	WEARABLE TECHNOLOGY AND APPLICATIONS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To provide a basic understanding of measurement systems and insight into sensors.
- To understand the concept of smart sensors.
- To identify the need for the development of wearable devices and their implications on various sectors.
- To gain knowledge on wearable IoT.
- To gain knowledge on applications of wearable technology in the field of healthcare.

UNIT I MEASUREMENTS AND SENSORS 9

Measurement System and Instruments, Applications and Classification of Instruments, Types of measured Quantities, Dispersion, Sample deviation and mean, Units and standards, Calibration and errors. Sensor systems, Transducers classification-sensors and actuators, General input-output configurations, Static and dynamic characteristics of measurement system.

UNIT II SMART SENSORS AND APPLICATIONS 9

Overview of various smart sensors: Digital temperature sensor, Humidity sensor, IR sensor, Gas sensor, Pressure sensors, Accelerometers, Flexible sensors.

UNIT III WEARABLE DEVICES 9

Emergence of wearable computing and wearable electronics, Types of wearable sensors: Invasive, Non-invasive; Intelligent clothing, sports, healthcare, Fashion and entertainment, military, environment monitoring, mining industry, public sector and safety.

UNIT IV WEARABLE IoT 9

Wearable IoT use cases- Smart watches, Android wear, Smart glasses, fitness trackers, health care devices, cameras, smart clothing etc

UNIT V WEARABLE TECHNOLOGY IN HEALTHCARE 9

Wearable Blood Pressure (BP) Measurement: Cuff-Based Sphygmomanometer, Cuffless Blood Pressure Monitor. Study of flexible and wearable Piezoresistive sensors for cuffless blood pressure measurement. Wearable sensors for Body Temperature: Intermittent and Continuous temperature monitoring-Detection principles.

TOTAL HOURS:45

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- Provide understanding of measurement systems and sensors.
- Analyze the concept of the smart sensors.
- Identify the need for development of wearable devices and its implications on various sectors.
- Familiarize about wearable IoT.
- Gain knowledge on applications of wearable technology in the field of healthcare.

REFERENCES:

1. Edward Sazonov, Michael R Neuman, "Wearable Sensors: Fundamentals, Implementation and Applications" Elsevier, 2014
2. "Wearable Sensors -Fundamentals, Implementation and Applications", by Edward Sazonov and Michael R. Neuman, Elsevier Inc., 2014.
3. "Wearable and Autonomous Biomedical Devices and Systems for Smart Environment", by Aimé Lay-Ekuakille and Subhas Chandra Mukhopadhyay, Springer 2010.
4. Alessandro Bassi, Martin Bauer, Martin Fiedler, Thorsten Kramp, Rob van Kranenburg, Sebastian Lange, Stefan Meissner, "Enabling things to talk – Designing IoT solutions with the IoT Architecture Reference Model", Springer Open, 2013
5. Toshiyo Tamura and Wenxi Chen, "Seamless Healthcare Monitoring", Springer 2018
6. Subhas Chandra Mukhopadhyay, "Wearable Electronics Sensors - For Safe and Healthy Living", Springer 2015

WEBSITE REFERENCES:

1. https://www.youtube.com/watch?v=CpDhjRX_WfA
2. https://www.hticiitm.org/wearables
3. https://jneuroengrehab.biomedcentral.com/articles/10.1186/1743-0003-9-21

JAE9002	INDUSTRIAL SAFETY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand mechanical, fire hazard fundamentals and safety management practices.
- To learn about chemical exposure, toxic radiations and industrial hygiene.
- To gain knowledge on environmental control, Industrial Noise and Health Hazards.
- To analyzeindustrial hazards and its risk assessment.
- Toknowsafety regulations

UNIT I INTRODUCTION 9

Evolution of modern safety concepts -Planning for safety for optimization of productivity– Fire prevention – Mechanical hazards – Boilers, Pressure vessels, Electrical Exposure.

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UNIT II CHEMICAL HAZARDS 9

Chemical exposure – Toxic materials – Ionizing Radiation and Non-ionizing Radiation - Industrial Hygiene – Industrial Toxicology

UNIT III ENVIRONMENTAL CONTROL 9

Industrial Health Hazards – Environmental Control – Industrial Noise - Noise measuring instruments, Control of Noise, Vibration, - Personal Protection..

UNIT IV HAZARD ANALYSIS 9

System Safety Analysis –Techniques – Fault Tree Analysis (FTA) - Failure Modes and Effects Analysis (FMEA)- HAZOP analysis and Risk Assessment

UNIT V SAFETY REGULATIONS 9

Explosions – Disaster management – catastrophe control, hazard control,Safety education and training - Factories Act - OSHA guidelines - Safety regulations Product safety – case studies.

COURSE OUTCOMES:

At the end of the course, the students will be able to:

- Apply the methods of prevention of fire and explosions.
- Analyze the effect of release of toxic substances and prevention from toxic exposure
- Estimate environmental noise and the controlling methods
- Understand the methods of hazard identification and preventive measures.
- Analyze and apply proper safety techniques on safety engineering and management.

REFERENCES:

1. John V.Grimaldi, "Safety Management", AITB S Publishers, 2003.
2. Safety Manual, "EDEL Engineering Consultancy", 2000.
3. David L.Goetsch, "Occupational Safety and Health for Technologists", 5th Edition, Engineers and Managers, Pearson Education Ltd., 2005.
4. Accident Prevention Manual for Industrial Operations NSC, Chicago, 1982.

WEBSITE REFERENCES:

1. https://www.osha.gov/sites/default/files/2019-03/fireprotection.pdf
2. https://www.osha.gov/chemical-hazards
3. https://www.youtube.com/watch?v=NJDgM-OFksw Acoustics and Noise control
4. https://www.mtu.edu/ehs/docs/hazard-analysis-instructions.pdf
5. https://www.youtube.com/watch?v=Yitx0SgLGPw Occupational Health and Safety Regulation and Guideline.

JAE9003	INTRODUCTION TO VLSI TECHNOLOGY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To learn the basic MOS Circuits ·
- To learn the MOS Process Technology ·
- To understand the design process of MOS devices.
- To design basic circuits using CMOS.
- To know about ASICs

UNIT 1 INTRODUCTION TO MOS TECHNOLOGY 9

Overview of VLSI Design Methodology VLSI design process- Basic MOS transistors- Enhancement mode transistor operation - Drain current Vs voltage derivation -NMOS inverter- Determination of pull up to pull down ratio for an NMOS inverter-CMOS inverter - DC Characteristics.

UNIT II VLSI FABRICATION TECHNOLOGY 9

An overview of wafer fabrication, oxidation, Photo Lithography, Diffusion, Ion implantation, Metallization, Packaging, nMOS process, n well CMOS process, p well CMOS process, Twin-Tub process, Silicon on insulator process.

UNIT III DESIGN PROCESS 9

VLSI Design Flow, MOS Layers, Stick diagram, Design rules, Layout generation, Fan- in and fan-out characteristics, Choice of layers, Introduction to scaling.

UNIT IV CMOS SUBSYSTEM DESIGN 9

Introduction, Alternative CMOS Logic structures, Design of Adders, Parity generators, One/Zero Detector, Comparators, Binary Counters, memory element.

UNIT V INTRODUCTION TO ASICs 9

Types, Standard Cell Array, Gate Arrays, Programmable Array Logic- PLAs, CPLDs, FPGAs.

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Learn the basics MOS Circuits ·
- Learn about MOS Process Technology ·
- Understand the design process of MOS devices.
- Design basic circuits using CMOS.
- Understand the basics about ASICs

REFERENCES:

1. Kamran Eshraghian, EshraghianDougles and A. Pucknell," Essentials of VLSI circuits and systems", PHI, 2005 Edition.
2. Weste and Eshraghian, "Principles of CMOS VLSI Design", Pearson Education, 1999.
3. John P. Uyemura, "Chip Design for Submicron VLSI: CMOS Layout &Simulation",Thomson Learning.
4. John.P. Uyemura, JohnWiley, "Introduction to VLSI Circuits and Systems",2003.
5. John M. Rabaey, "Digital Integrated Circuits" PHI, EEE, 1997.
6. Wayne Wolf, "Modern VLSI Design" Pearson Education.

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1. https://nptel.ac.in/courses/117101058
2. https://archive.nptel.ac.in/courses/108/101/108101089/#
3. https://www.learnelectronicsindia.com/post/design-flow-of-vlsi-technology
4. https://www.youtube.com/watch?v=vUnKDl8M_QM
5. https://freevideolectures.com/subject/vlsi-and-asic-design/

JAE9004	INTRODUCTION TO EMBEDDED CONTROLLERS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the basics of Embedded System
- To understand about the hardware and peripheral requirements of embedded system
- To gain knowledge about selection of microcontroller
- To understand the concepts of RTOS
- To study various applications in embedded design

UNIT 1 INTRODUCTION 9

Embedded Systems and general purpose computer systems, history, classifications, applications and purpose of embedded systems.

UNIT II EMBEDDED HARDWARE AND PERIPHERALS 9

Embedded Hardware: Memory map, i/o map, interrupt map, processor family, external peripherals, memory – RAM, ROM, types of RAM and ROM, memory testing, CRC,Flash memory. **Peripherals:** Control and Status Registers, Device Driver, Timer Driver - Watchdog Timers.

UNIT III EMBEDDED SYSTEM WITH 8051 MICROCONTROLLER 9

Factors to be considered in selecting a controller, why 8051 Microcontroller, Designing with 8051.Structure of embedded program, infinite loop, compiling, linking and debugging.

UNIT IV REAL TIME OPERATING SYSTEM (RTOS) 9

Full Scan DFT Technique, Scan Architectures and RT Level Scan Design - Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, RT Level Boundary Scan and Boundary Scan Description Language - Logic Built-in Self-test: BIST Basics.

UNIT V CASE STUDIES 9

Design using Embedded System: Application specific – washing machine, Digital Camera; domain specific – automatic vending machine, train controller.

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Learn the basics of Embedded System
- Analyze the hardware and peripheral requirements of embedded system
- Analyze about selection of microcontroller
- Gain knowledge about the concepts of RTOS
- Study various applications in embedded design

REFERENCES:

1. Shibu K V, Introduction to Embedded Systems, Tata Mcgraw-Hill, 1st Edition, June 2012.
2. Muhammad Ali Mazidi, The 8051 Microcontroller and Embedded Systems, Pearson, 2nd edition, 2011.
3. Rajkamal, Embedded Systems: Architecture, Programming and Design,Tata Mcgraw-Hill, 2nd Edition, December 2008.
4. Michael Barr, Programming Embedded Systems in C and C++,O'Reilly Media, Inc. 1st Edition, 1999.

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2. https://nptel.ac.in/courses/108102169.
3. http://nptel.ac.in/courses/108102045/28
4. http://nptel.ac.in/courses/108102045
5. https://www.windriver.com/solutions/learning/rtos

JAE9005	AUTOMATIVE ELECTRONICS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the basics of electronic engine control
- To understand sensors and actuators in automobiles
- To gain knowledge about the digital engine control system
- To understand the concepts of automotive networking
- To study various future automotive electronic systems

UNIT I BASICS OF ELECTRONIC ENGINE CONTROL 9

Introduction to Electronic systems in Automotives, Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Effect of Air/Fuel ratio, spark timing, Control Strategy, Electronic Fuel control system, Electronic Ignition.

UNIT II SENSOR AND ACTUATORS IN AUTOMOTIVES 9

Working principle and characteristics of Airflow rate, Engine crankshaft angular position, Hall effect, Throttle angle, temperature, exhaust gas oxygen sensors – study of fuel injector, exhaust gas recirculation actuators, stepper motor actuator, vacuum operated actuator.

.

UNIT III DIGITAL ENGINE CONTROL SYSTEMS 9

Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Automatic System Adjustment, System Diagnostics Digital modules in the Control unit.

UNIT IV AUTOMOTIVE NETWORKING 9

Bus Systems–Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, FlexRay, Diagnostic Interfaces.

UNIT V FUTURE AUTOMOTIVE ELECTRONIC SYSTEMS 9

Architecture for vision system-Features-applications -image processing –Speech Synthesis, Navigation – Navigation Sensors, Intelligent robot vehicles – obstacle detection, collision warning and avoidance system.

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- To analyze the basics of electronic engine control
- To select sensors and actuators in automobiles
- To analyze digital engine control system
- To analyze the concepts of automotive networking
- To explore various future automotive electronic systems

REFERENCES:

1. Ribbens, “Understanding Automotive Electronics”, 8th Edition, Elsevier, Indian Reprint, 2013
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley& Sons Inc., 2007.
3. Najamuz Zaman , “ Automotive Electronics Design Fundamental’’ first edition, Springer 2015.

WEBSITE REFERENCES:

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2. https://archive.nptel.ac.in/courses/107/106/107106088/
3. https://archive.nptel.ac.in/courses/107/106/107106088/
4. https://onlinecourses.nptel.ac.in/noc22_de02/preview
5. https://onlinecourses.nptel.ac.in/noc21_ee32/preview

NON CREDIT MANDATORY COURSES (NCM)

JNC5001	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING 6

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS 6

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title
- Understand the skills needed when writing the Conclusion
- Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press(available on Google Books)2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

JNC5002	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics.

UNIT IV DISASTER PREPAREDNESSAND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment Strategies for Survival.

TOTAL: 30 PERIODS

-COURSE OUTCOMES:

At the end of the course, Students will be able to

- Ability to summarize basics of disaster
- Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. GoelS.L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt.Ltd., New Delhi, 2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "New Royal book Company,2007.
3. Sahni, Pardeep Et.Al.,"Disaster Mitigation Experiences And Reflections" ,Prentice Hall of India, New Delhi,2001.

JNC5003	SANSKRIT FOR TECHNICAL KNOWLEDGE	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Illustrate the basic sanskrit language.
- Recognize sanskrit, the scientific language in the world.
- Appraise learning of sanskrit to improve brain functioning.
- Relate sanskrit to develop the logic in mathematics, science & other subjects enhancing them memory power.
- Extract huge knowledge from ancient literature.

UNIT I ALPHABETS **6**

Alphabets in Sanskrit

UNIT II TENSES AND SENTENCES **6**

Past/Present/ Future Tense-Simple Sentences

UNIT III ORDERAND ROOTS **6**

Order-Introduction of roots

UNIT IV SANSKRIT LITERATURE **6**

Technical information about Sanskrit Literature

UNIT V TECHNICAL CONCEPTSOF ENGINEERING **6**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Understanding basic Sanskrit language.
- Write sentences.
- Know the order and roots of Sanskrit.
- Know about technical information about Sanskrit literature.
- Understand the technical concepts of Engineering.

REFERENCES:

1. "Abhyaspustakam"–Dr.Vishwas,Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" PrathamaDeeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam,New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi,2017.

JNC5004	VALUE EDUCATION	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Understand value of education and self-development
- Imbibe good values in students
- Let them know about the importance of character
- Students can develop good habits

UNIT I **6**

Values and self-development–Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non moral valuation. Standards and principles, Value judgements.

UNIT II **6**

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance, Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity, Patriotism, Love for nature, Discipline.

UNIT III **6**

Personality and Behavior Development-Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brother hood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

UNIT IV **6**

Character and Competence–Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

REFERENCES:

1. Chakroborty,S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

JNC5005	CONSTITUTION OF INDIA	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional Role and entitlement to civil and economic rights as well as the emergence nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION 6

History, Drafting Committee, (Composition &Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION 3

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES 6

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE 6

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION 6

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION 3

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners -Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the frame work of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

REFERENCES:

1. The Constitution of India,1950 (Bare Act),Government Publication.
2. Dr.S.N.Busi,Dr.B.R.Ambedkar framing of Indian Constitution,1st Edition,2015.
3. M.P.Jain, Indian Constitution Law,7th Edn., LexisNexis,2014.
4. D.D.Basu, Introduction to the Constitution of India,LexisNexis,2015.

JNC5006	PEDAGOGY STUDIES	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Review existing evidence on their view topic to inform programme design and policy
- Making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

UNIT I INTRODUCTION AND METHODOLOGY: 6

Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education-Conceptual framework, Research questions-Overview of methodology and Searching.

UNIT II THEMATIC OVERVIEW 6

Pedagogical practices are being used by teachers in formal and in formal classrooms in developing countries-Curriculum, Teacher education.

UNIT III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES 6

Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV PROFESSIONAL DEVELOPMENT 6

Professional development: alignment with classroom practices and follow up support - Peer support - Support from the head teacher and the community - Curriculum and assessment -Barriers to learning: limited resources and large class sizes.

UNIT V RESEARCH GAPS AND FUTURE DIRECTIONS 6

Research design–Contexts–Pedagogy-Teacher education -Curriculum and assessment-Dissemination and research impact.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare,31(2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies,36(3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana-does it count? Multi-site teacher education research project (MUSTER)countryreport1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count?
5. International Journal Educational Development, 33(3):272–282.Alexander R J (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A massscale, rapid, 'learning to read 'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf

JNC5007	STRESS MANAGEMENT BY YOGA	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- To achieve overall health of body and mind
- To overcome stress

UNIT I **10**

Definitions of Eight parts of yoga (Ashtanga)

UNIT II **10**

Yam and Niyam-Do`s and Don't's in life -i)Ahinsa,satya,astheya, bramhacharya and aparigraha, ii)Ahinsa,satya,astheya,bramhacharya and aparigraha.

UNIT III **10**

Asanand Pranayam-Various yoga poses and their benefits for mind & body-Regularization of breathing techniques and its effects-Types of pranayam

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Develop healthy mind in a healthy body thus improving social health
- Improve efficiency

REFERENCES:

1. 'Yogic Asanas for Group Training -Part-I": Janardan Swami Yoga bhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department),Kolkata

JNC5008	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

UNIT I **10**

Neetisatakam- holistic development of personality - Verses- 19,20,21,22 (wisdom) - Verses-29,31,32 (pride & heroism) – Verses- 26,28,63,65 (virtue) - Verses- 52,53,59 (dont's) - Verses-71,73,75,78(do's)

UNIT II **10**

Approach to day today work and duties-Shrimad Bhagwad Geeta: Chapter2-Verses41,47,48-Chapter3-Verses13,21,27,35Chapter6-Verses5,13,17,23,35-Chapter18-Verses
45,46,48.

UNIT III **10**

Statements of basic knowledge-Shrimad Bhagwad Geeta: Chapter2-Verses 56,62,68 Chapter12-Verses13,14,15,16,17,18-Personality of role model-shrimad bhagwadgeeta- Chapter2- Verses17, Chapter3-Verses 36,37,42-Chapter4-Verses18,38,39 Chapter18—
Verses37,38, 63

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students.

REFERENCES:

1. Gopinath, Rashtriya Sanskrit SansthanamP ,Bhartrihari's Three Satakam, Niti-sringar-vairagya, New Delhi,2010
2. Swami Swarupananda, Srimad Bhagavad Gita, Advaita Ashram, Publication Department, Kolkata, 2016.