JEC1402

LINEAR INTEGRATED CIRCUITS

OBJECTIVES

- To introduce the basic building blocks of linear integrated circuits
- To learn the linear and non-linear applications of operational amplifiers
- To introduce the theory and applications of analog multipliers and PLL
- To learn the theory of ADC and DAC
- To introduce the concepts of waveform generation and introduce some special function ICs

OUTCOMES

At the end of the course, the student should be able:

- To design linear and non linear applications of OP – AMPS
- To design applications using analog multiplier and PLL
- To design ADC and DAC using OP – AMPS
- To demonstrate waveforms using OP – AMP Circuits
- To analyze special function ICs

TEXT BOOKS:

1. D.Roy Choudhry, Shail Jain, “Linear Integrated Circuits”, New Age International Pvt. Ltd., 2018, Fifth Edition.
2. Ramakant A. Gayakwad, “OP-AMP and Linear ICs”, 4th Edition, Prentice Hall / Pearson Education, 2015.

REFERENCES:

1. Robert F.Coughlin, Frederick F.Driscoll, “Operational Amplifiers and Linear Integrated Circuits”, Sixth Edition, PHI, 2001.
2. B.S.Sonde, “System design using Integrated Circuits”, 2nd Edition, New Age Pub, 2001
3. Sergio Franco, “Design with Operational Amplifiers and Analog Integrated Circuits”, 4th Edition, Tata McGraw-Hill, 2016
4. Gray and Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley International, 5th Edition, 2009

NEW AGE

LINEAR INTEGRATED CIRCUITS

FOURTH
Multi Colour
EDITION

D. Roy Choudhury
Shail B. Jain

NEW AGE INTERNATIONAL PUBLISHERS

UNIT I

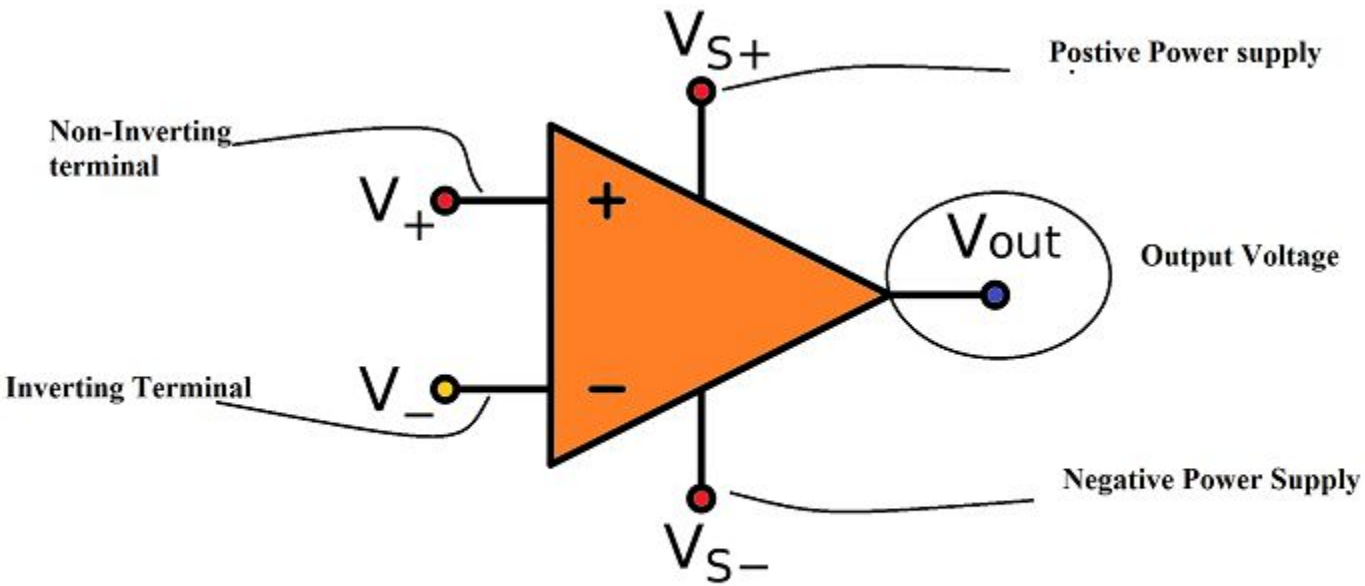
BASICS OF OPERATIONAL AMPLIFIERS

Operational Amplifier and its characteristics - General operational amplifier stages - Internal circuit diagram of IC 741 - DC and AC performance characteristics, slew rate, CMRR - Open and closed loop configurations-Sign Changer, Scale Changer, Voltage Follower.

Operational Amplifier(IC741)

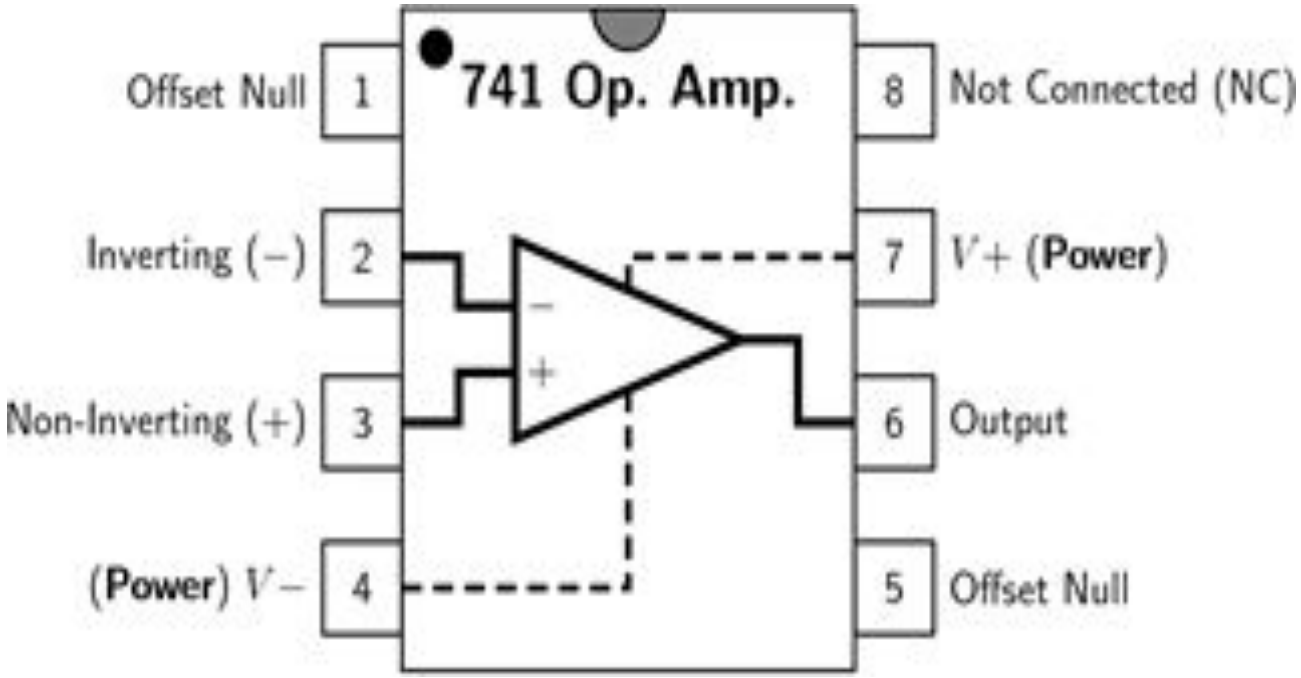
- An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
- It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

Operational Amplifier Symbol



Operational Amplifier Symbol

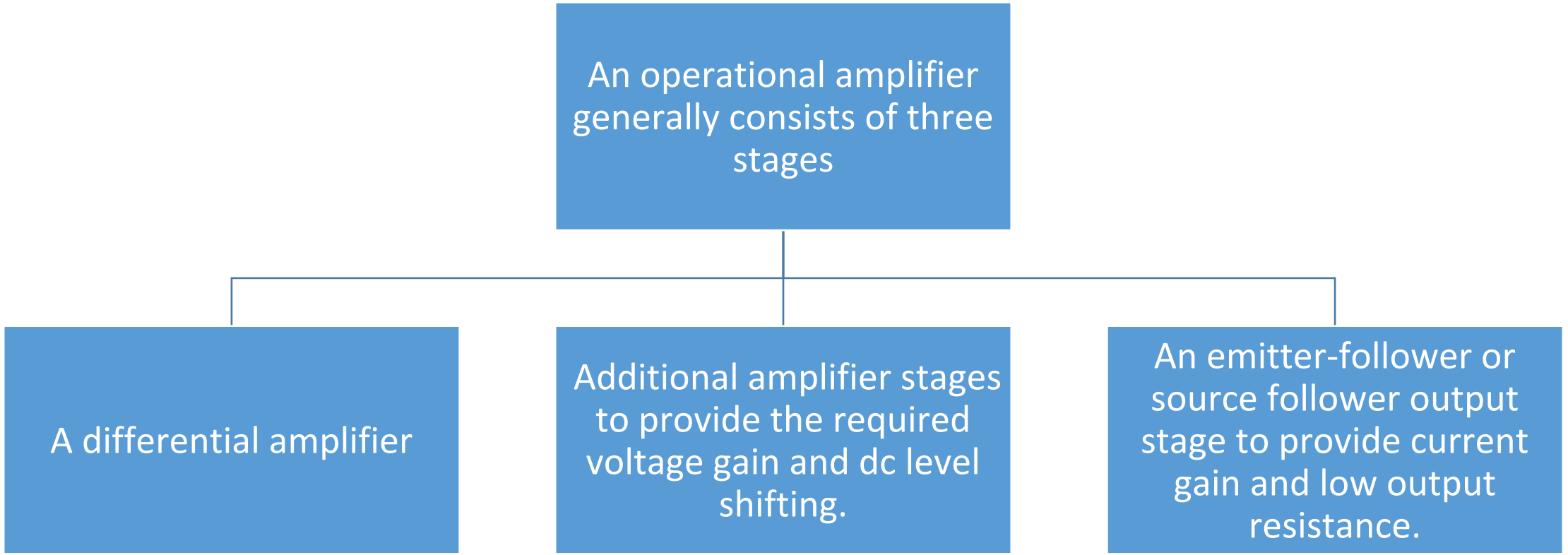
PIN DIAGRAM


741 Op. Amp.
Offset Null
1
Inverting (−)
2
Non-Inverting (+)
3
(Power) V−
4
8
Not Connected (NC)
7
V+ (Power)
6
Output
5
Offset Null
−
+

Ideal op-amp characteristics

- Infinite voltage gain A.
- Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.
- Zero output resistance Ro, so that the output can drive an infinite number of other devices.
- Zero output voltage, when input voltage is zero.
- Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
- Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

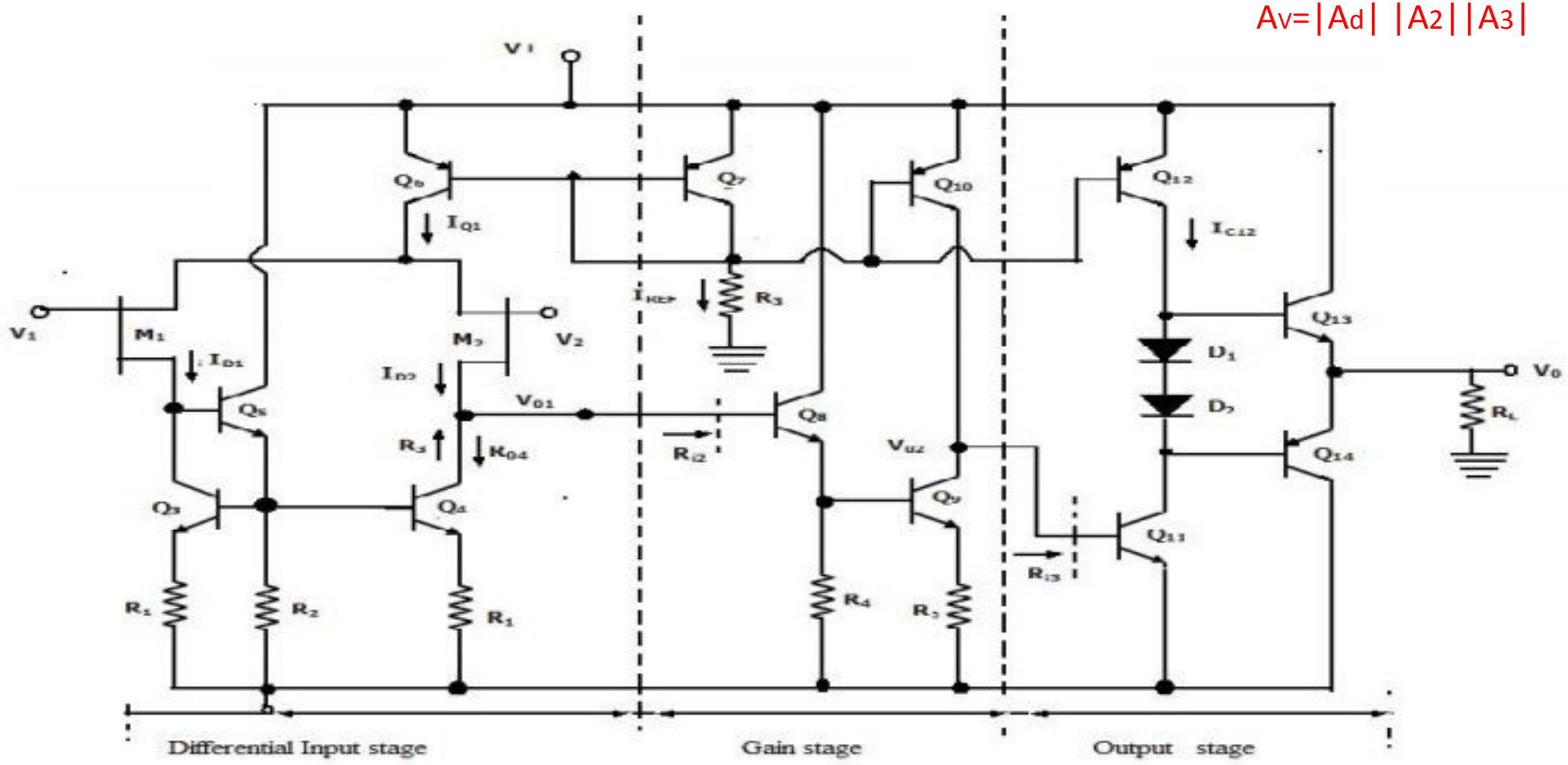
General Operational Amplifier stages



- A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp.
- The output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage.
- Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed.
- Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

General operational amplifier stages

$A_V = |A_d|\ |A_2|\ |A_3|$



Input stage

- The input differential amplifier stage uses p-channel JFETs M1 and M2. It employs a three transistor active load formed by Q3, Q4, and Q5.
- The bias current for the stage is provided by a two-transistor current source using PNP transistors Q6 and Q7.
- Resistor R1 increases the output resistance seen looking into the collector of Q4 as indicated by R04. This is necessary to provide bias current stability against the transistor parameter variations.
- Resistor R2 establishes a definite bias current through Q5.
- A single ended output is taken out at the collector of Q4. MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage

- The second stage or the gain stage uses Darlington transistor pair formed by Q8 and Q9 as shown in figure.
- The transistor Q8 is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage.
- The transistor Q9 provides an additional gain and Q10 acts as an active load for this stage.
- The current mirror formed by Q7 and Q10 establishes the bias current for Q9.
- The VBE drop across Q9 and drop across R5 constitute the voltage drop across R4, and this voltage sets the current through Q8.
- It can be set to a small value, such that the base current of Q8 also is very less.

Output stage

- The final stage of the op-amp is a class AB complementary push-pull output stage.
- Q11 is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage.
- Bias current for Q11 is provided by the current mirror formed by Q7 and Q12, through Q13 and Q14 for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.
- The overall voltage gain AV of the op-amp is the product of voltage gain of each stage as given by

$$A_V = |A_d| \; |A_2| \, |A_3|$$

Where ,Ad is the gain of the differential amplifier stage, A2 is the gain of the second gain stage and A3 is the gain of the output stage.